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Synthetic Instruments an overview

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- IEEE Standards
- Defense Industry
- Synthetic & Virtual Instrument
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- Questions

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Introduction

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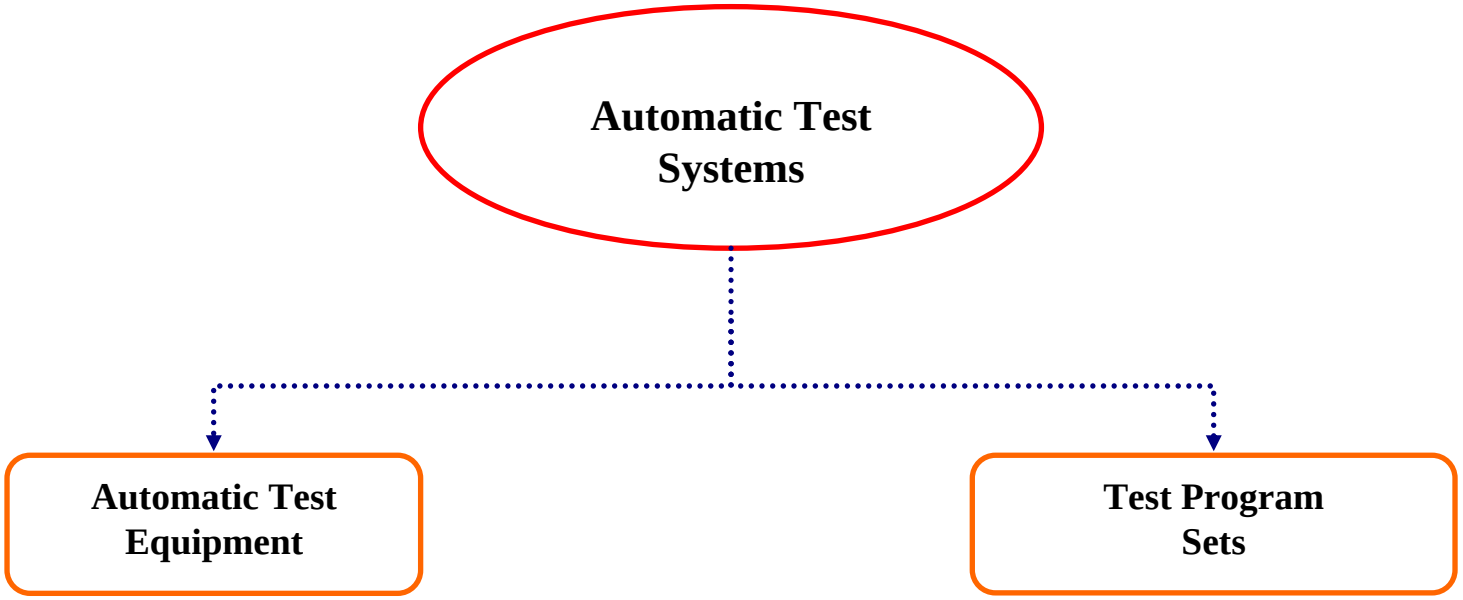
Synthetic Measurement System

A synthetic measurement system (SMS) is a system that uses synthetic instruments implemented on a common, general purpose, physical hardware platform to perform a set of specific measurements using numeric processing techniques.

Synthetic Instruments

A synthetic instrument is a functional mode or personality component of an SMS that performs specific synthesis or analysis function using specific software running on generic, non-specific physical hardware.



- **GPIB**
- **VMEbus**
- **PCIbus**

Can be configured to Test

- Black Boxes (such as LRU's or WRA)
- Circuit Cards (such as SRU or SRA)

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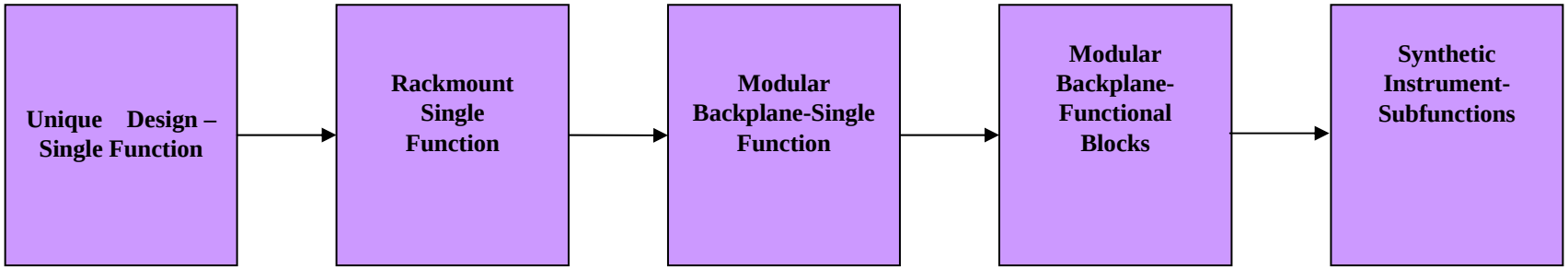
Automatic Test Systems



- Cost and product availability
- Development expenses
- Long term support

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Design Requirements

Requirement	Goal
Size	**Minimum Size**
Power Requirements	**Portable, Battery operation**
Modularity	**Low level functions**
Interface Bandwidth	**Utilize Existing Bus**
Processing Power	**Leverage PC Architecture**
Reliability	**Increased MTBF**
Upgrade Capability	**Block Level**
Cost	**Reduced**

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IEEE Standards

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- Formal Standards
- De Facto Standards
- Evolving Standards

Standards

Formal	De Facto	Evolving
IEEE-488	PXI	LXI
VXI (IEE-1155)	IVI	IEEE-P1552: Structured Architecture for Test Systems
IEEE-1641	TYX PAWS	
IEEE-716 ATLAS		IEEE-P1505
IEEE-1671		IEEE-P1505.1
IEEE-P1232a		IEEE-1149
IEEE-P1636.1		
IEEE-P1671.1		
IEEE-P1671.2		

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Defense Industry

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Demands of DoD market

- Reduce the total cost of ownership of the ATS
- Reduce time to develop and field new or upgraded ATSs
- Provide greater flexibility between the US and coalition partners through interoperable ATSs
- Reduce test system logistics footprint
- Reduce the test systems physical footprint

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Synthetic & Virtual Instruments

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Virtual Instrumentation

The concept of Virtual Instrumentation (VI) was developed within the Interchangeable VI foundation. It is defined as a software- defined system where software based on user requirements defines the functionality of generic measurement hardware i.e. it is a combination of hardware and software into a reusable building blocks, where the results are presented on a computer screen rather than on a display with the intention to create maximum flexibility.

A VI system may be used in a design or R&D lab as well as in production testing. Dependent on the application, the focus may shift on how the system is accessed by the user. The user could be accessing, for example, a test program or a standalone GUI. Note here, that the GUI is not in general a part of the VI system, but a user of this system.

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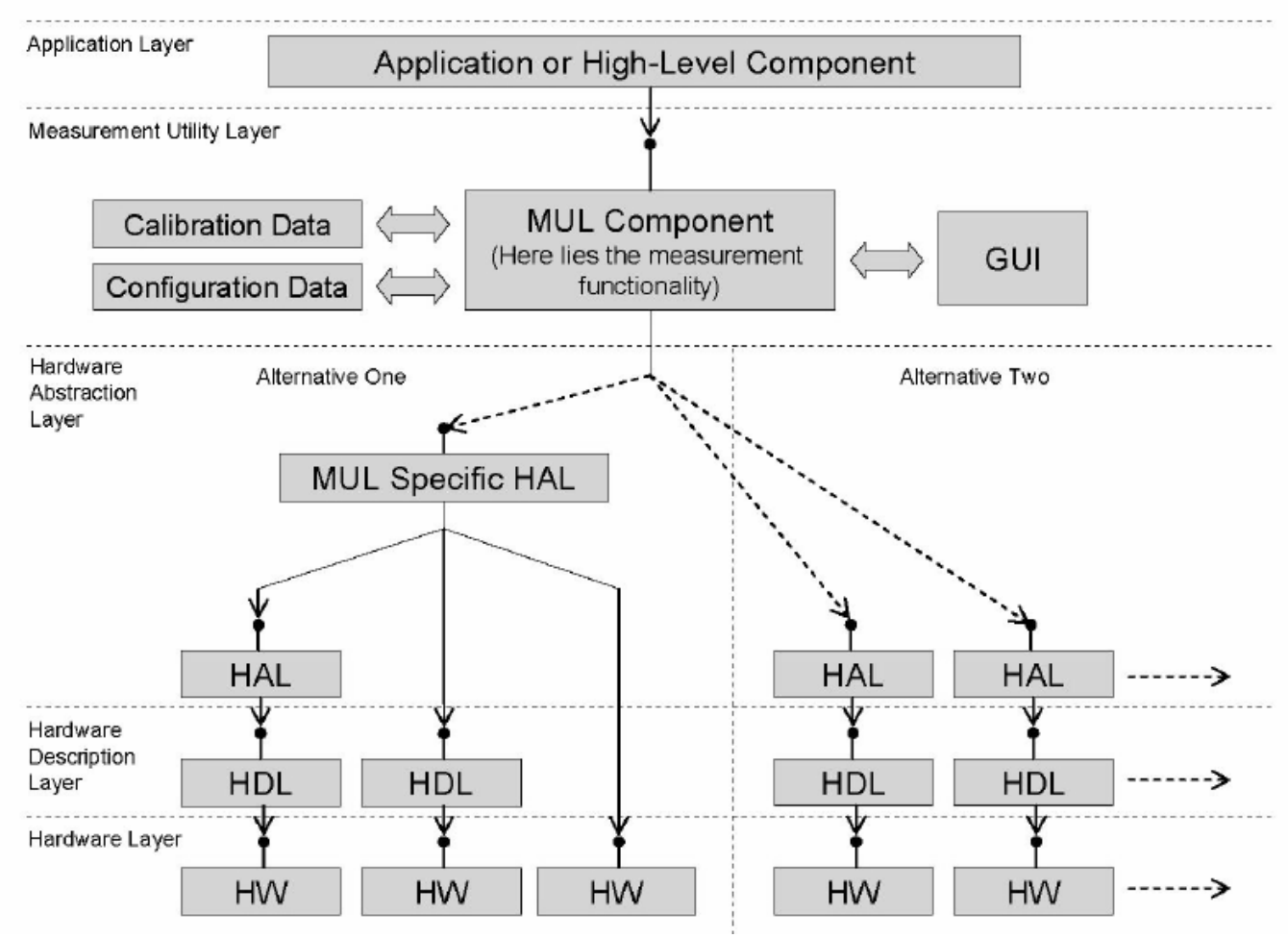
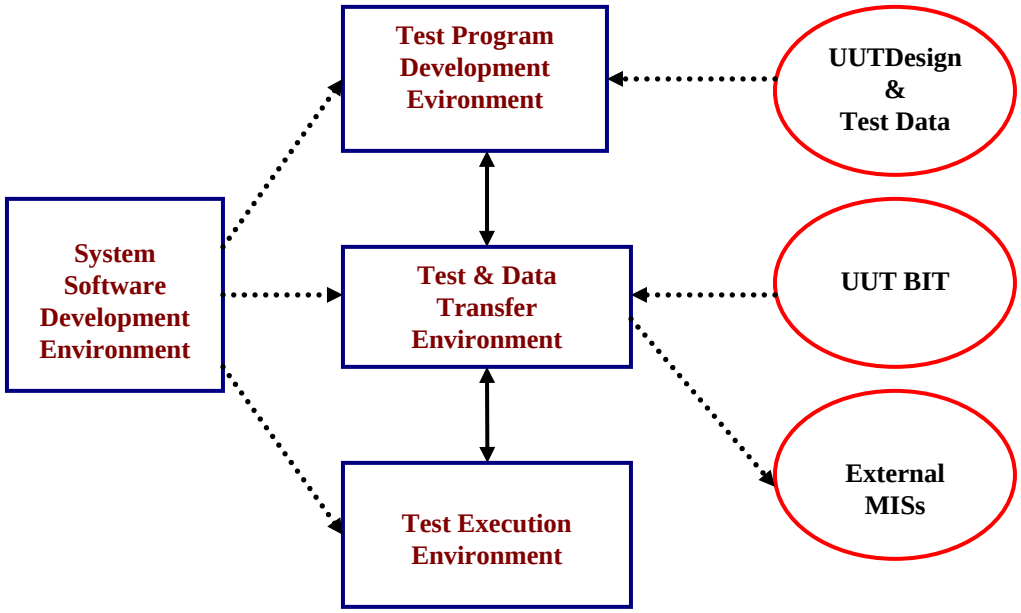
Software Structure



NxTest software architecture



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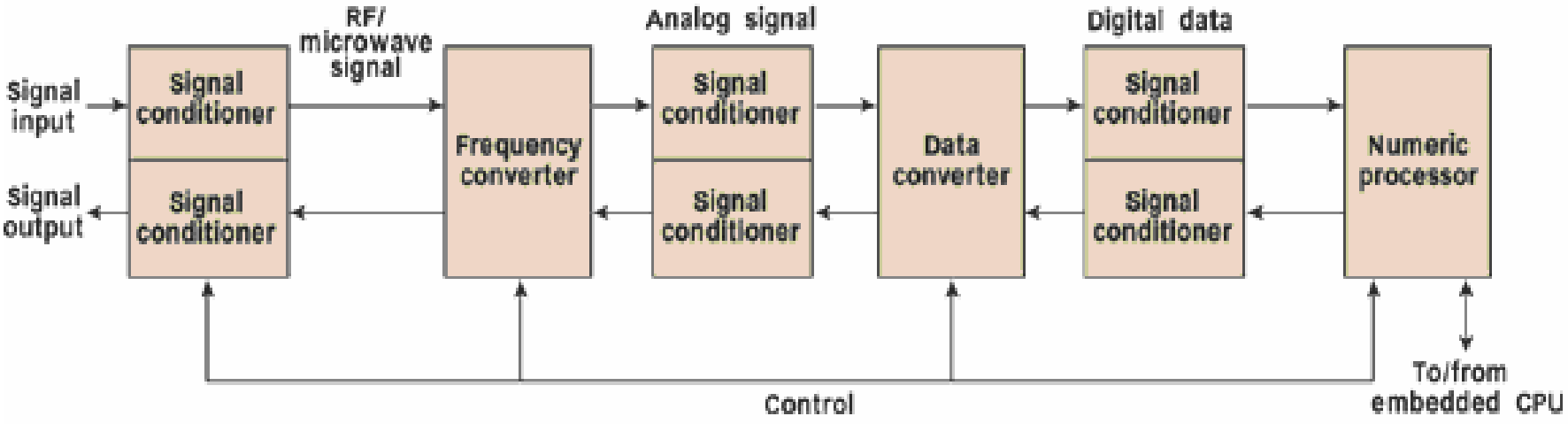
Synthetic Instrument Architecture



- Signal Conditioners
- Frequency Converters
- Data Converters
- Numeric Processor
- Data Processor / Controller

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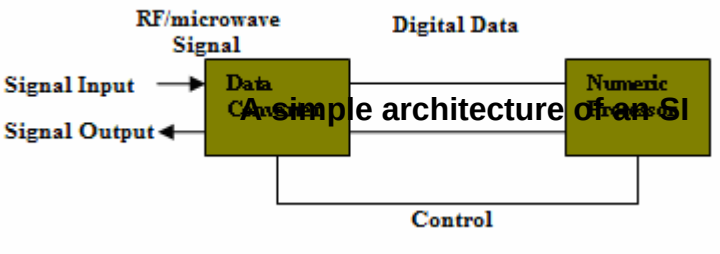
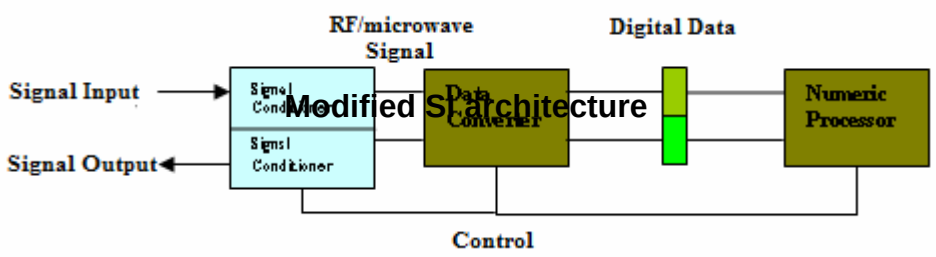
Simple Model



A simple architecture of an SI



Modified SI architecture

Wanted Signals	Unknown Signals
Frequency Range	Spurious Signals
Signal to Noise Ratio	Distortion Products
Modulation B/W (time varying)	Thermal (noise)
Power Range (sensitivity)	Interference (EMI)

The key issues for known and unknown signals

$$ENOB = \frac{SNR_A - 1.76dB - 10\log(f_s / 2f_a)}{6.02}$$

$$where: SNR_A = 20\log\left(\frac{RMS\ \ Signal\ \ Level}{RMS\ \ noise\ \ level}\right)$$

f_S = sampling rate ; f_a = analog bandwidth

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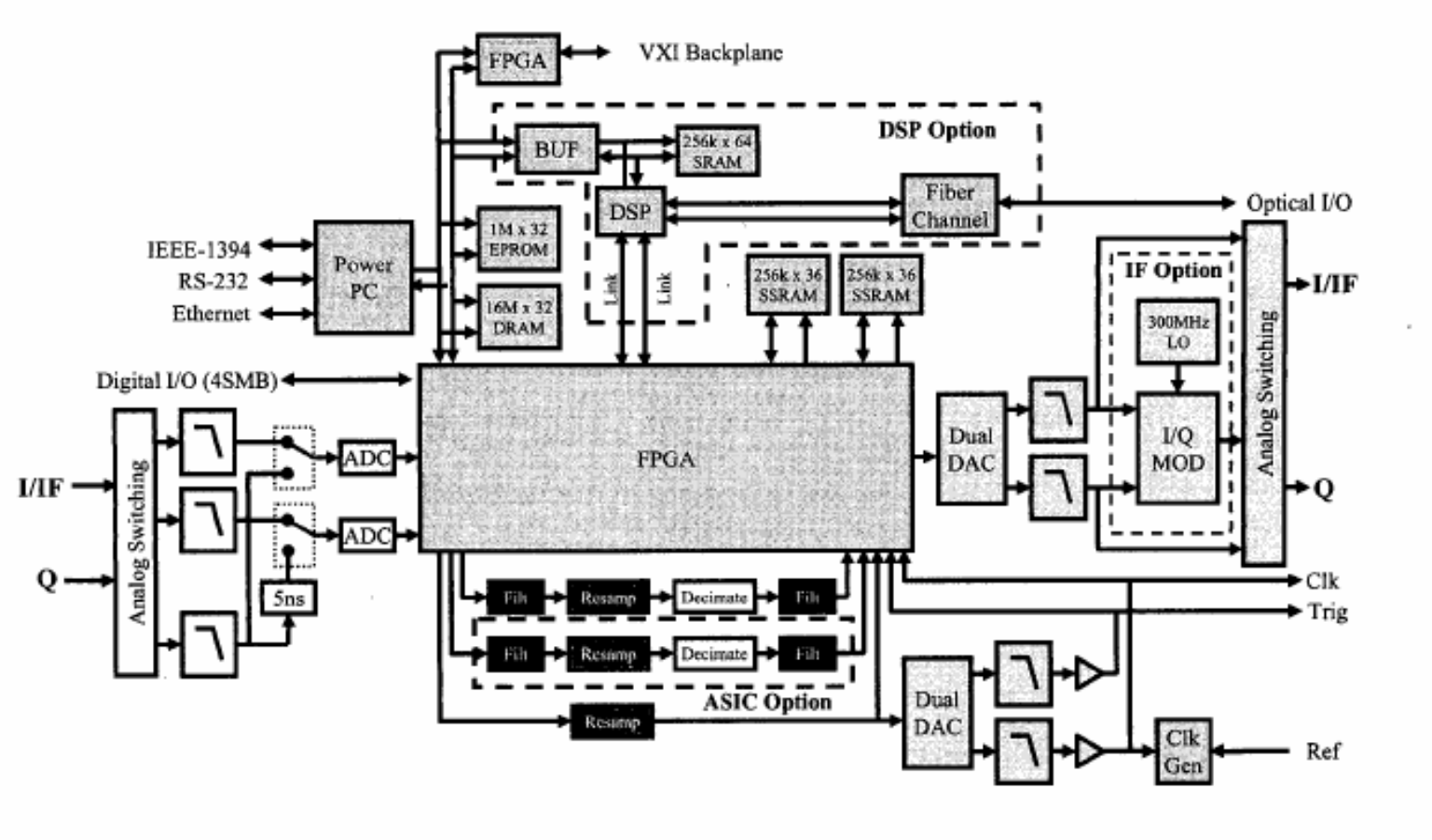
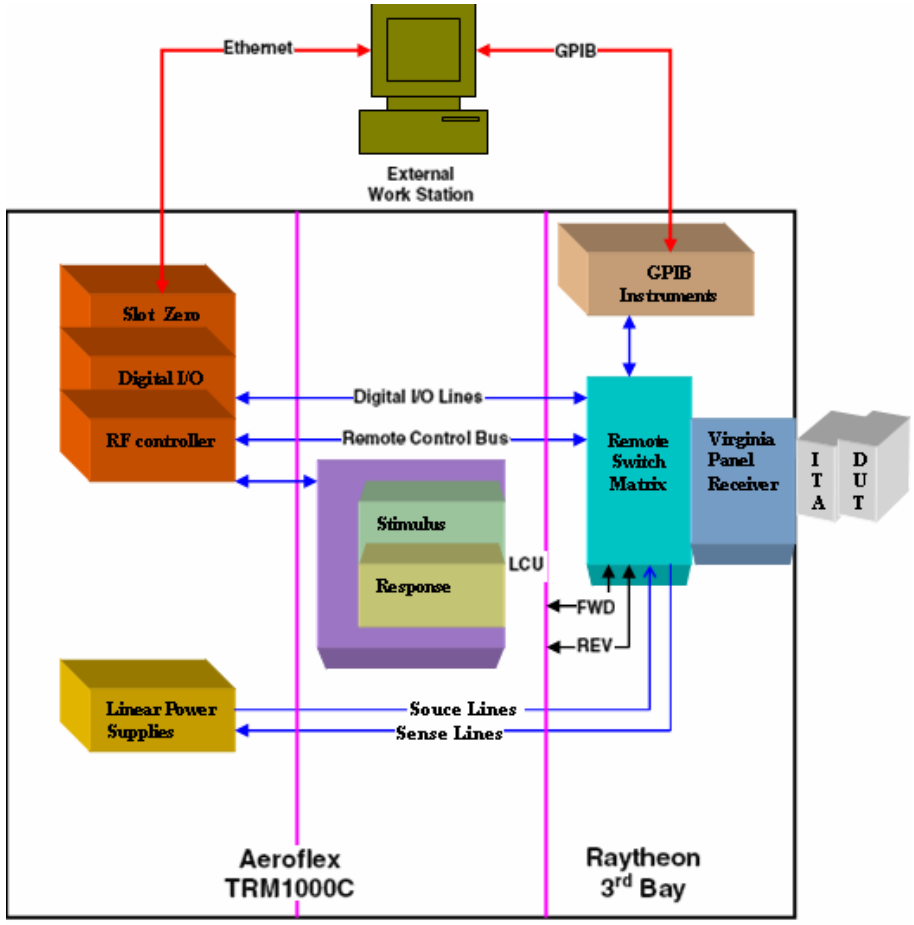
Synthetic Wideband Instrument Architecture



TRM 1000C


Ethernet
GPIB
External
Work Station
GPIB
Instruments
Slot Zero
Digital I/O
RF controller
Digital I/O Lines
Remote Control Bus
Remote
Switch
Matrix
Virginia
Panel
Receiver
I
T
A
D
U
T
Stimulus
Response
LCU
FWD
REV
Linear Power
Supplies
Souce Lines
Sense Lines
Aeroflex
TRM1000C
Raytheon
3rd Bay

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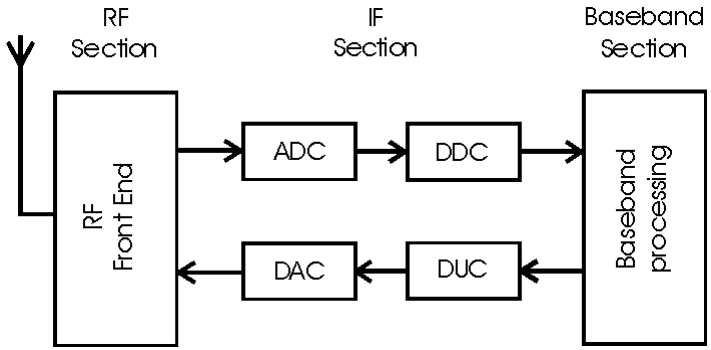
Software Defined Radios (SDR)



- **DSP**
- **FPGA**
- **GPP**

Implements the radio functionality to transmit and receive signals

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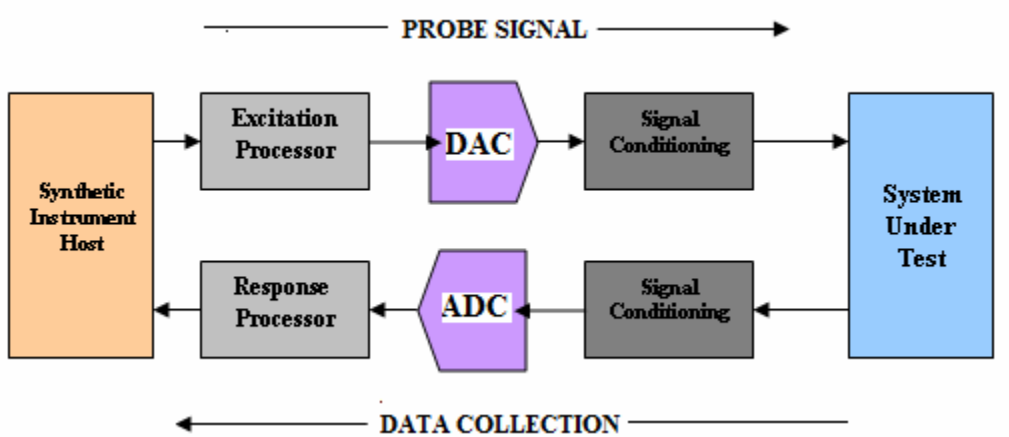
Coupled Data Collection Units



- Analog signal conditioning unit,
- ADC, and the
- Signal-processing unit.

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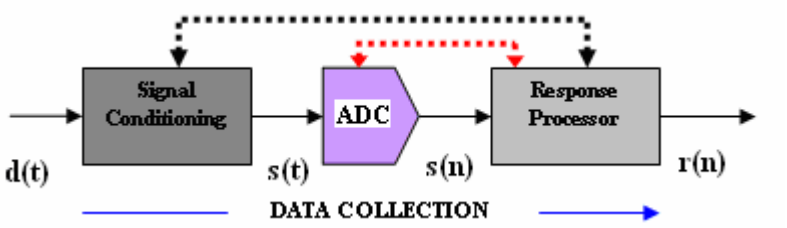
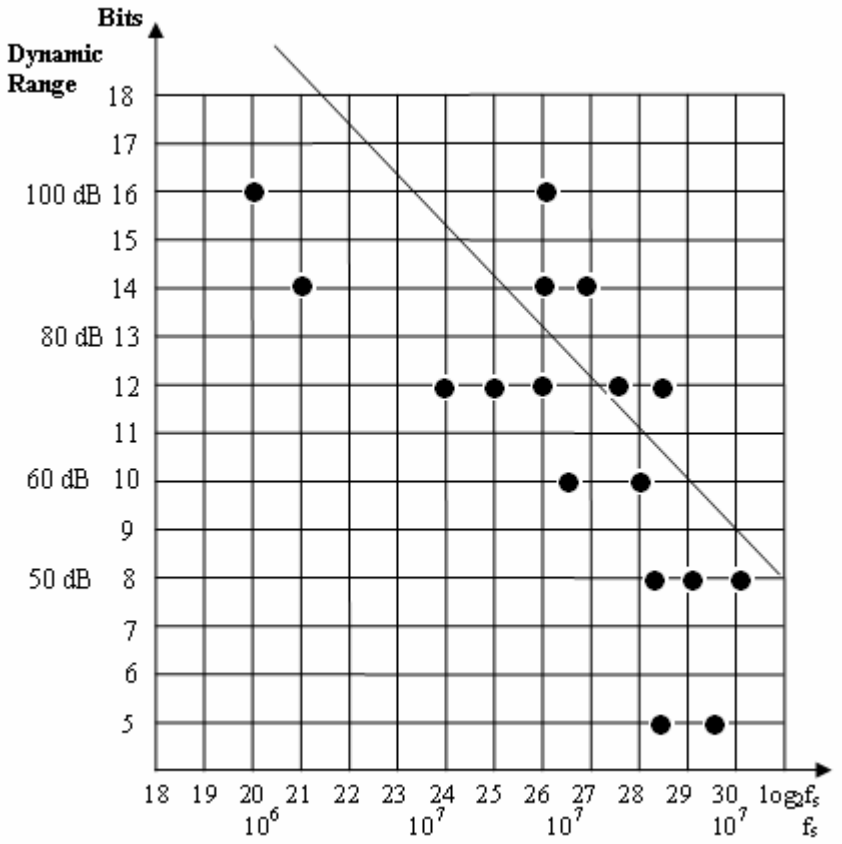
ADC & DAC Technology



$$\log_2(2^k f_{SAMPLE}) = k$$

$$b = \log_2(k) - \log_2(f_{SAMPLE})$$



Number of Bits	Sample Rate	SNR	SFDR
8	1.5 GHz	47 dB	54 dB
12	200 MHz	65 dB	80 dB
16	1 MHz	94 dB	110 dB
20	24 kHz	112 dB	112 dB

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Signal Conditioning

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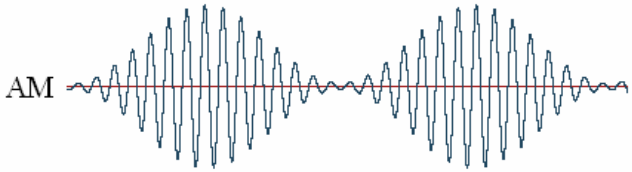
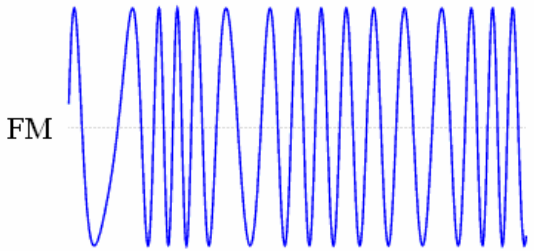
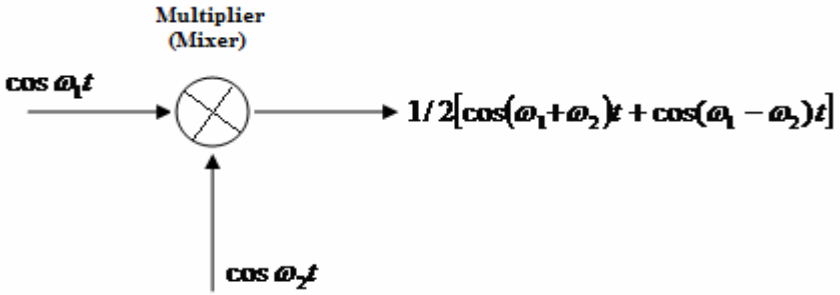
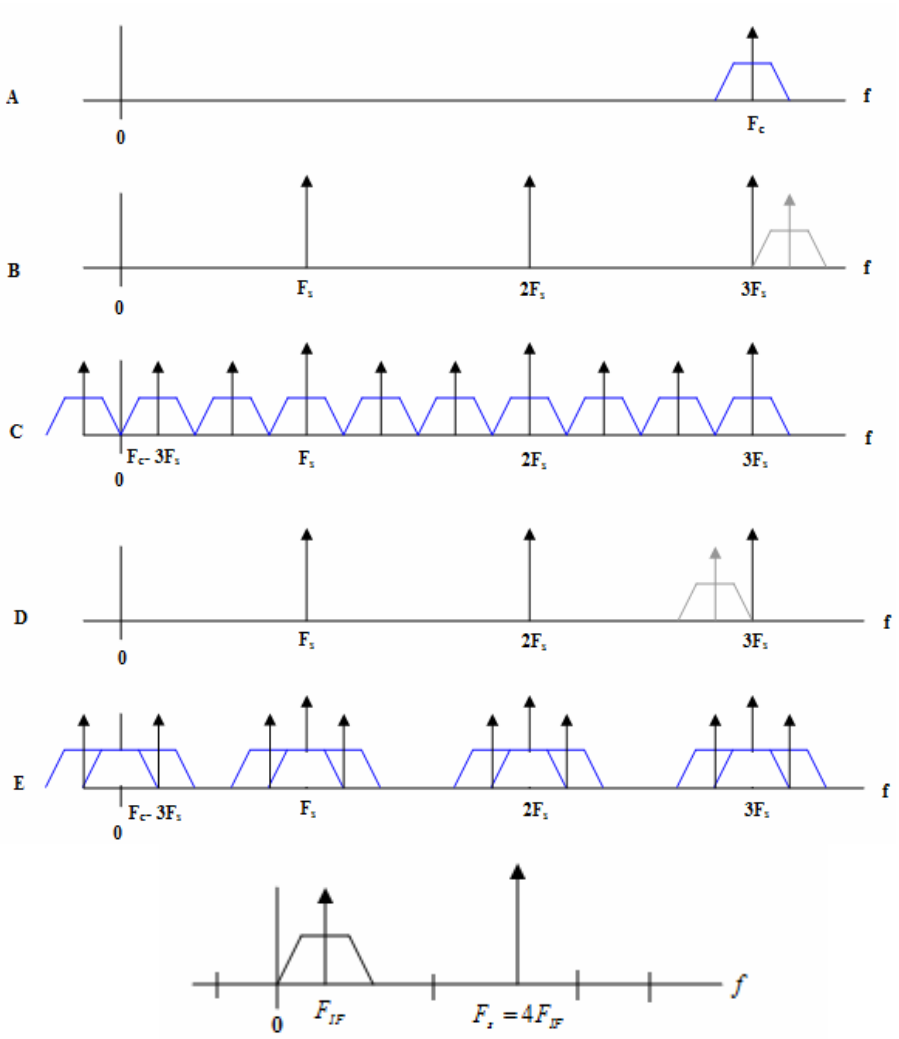
Sampling

- **Bandpass Sampling**
- **I/Q Sampling**









The sampling rate is Fs and is illustrated with harmonics of Fs shown as impulses out at Fs multiples: Fs, 2Fs, 3Fs ….

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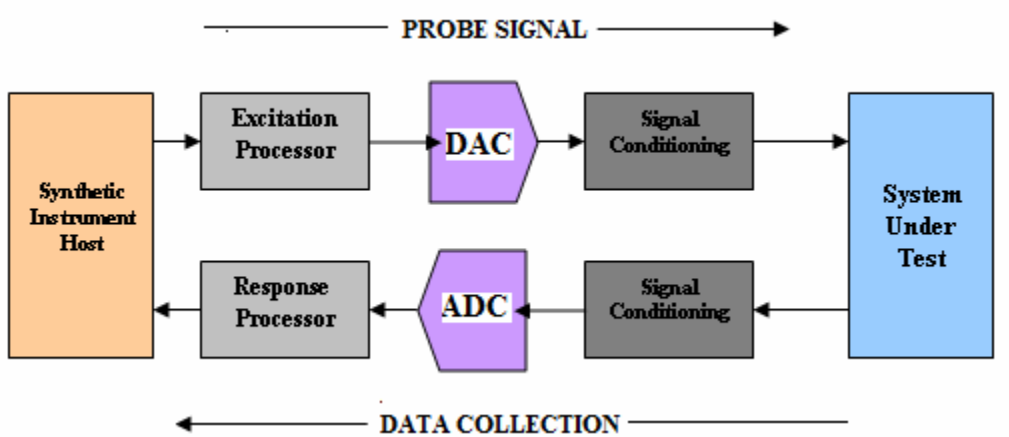
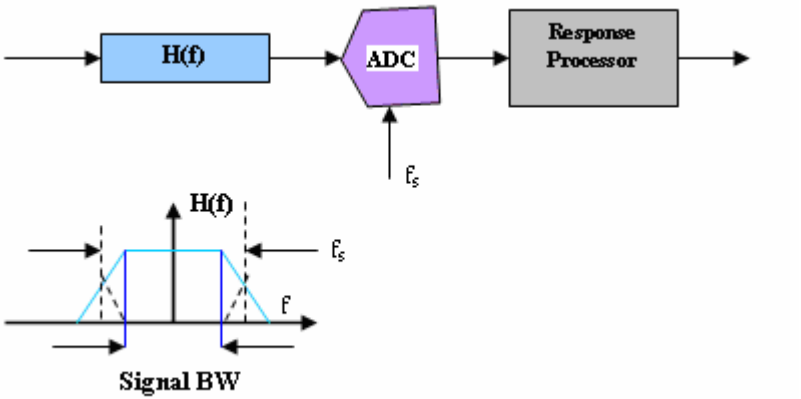
Coupled Data Collection Units



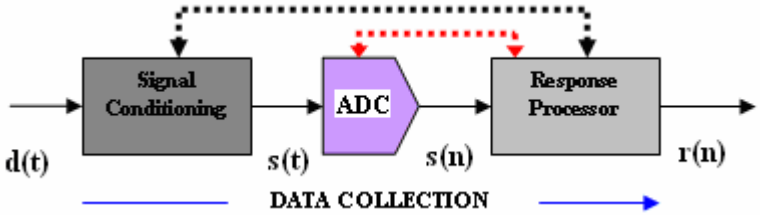
- Analog signal conditioning unit,
- ADC, and the
- Signal-processing unit.

Option-1

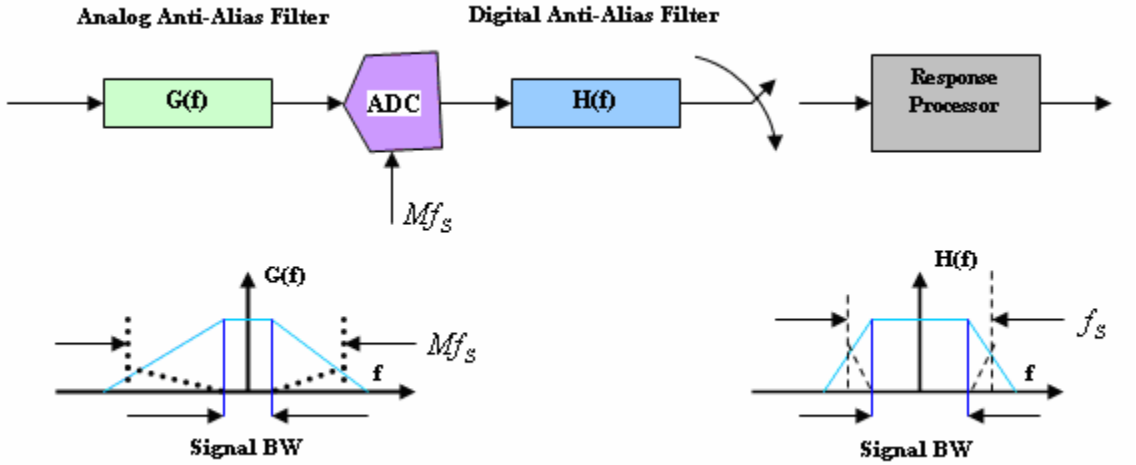


$$f_{SAMPLE} = 2sided\ BW + \Delta f$$

$$\Delta f = Transition\ \ BW\ \ of\ \ Anti-Alias\ \ Filter$$

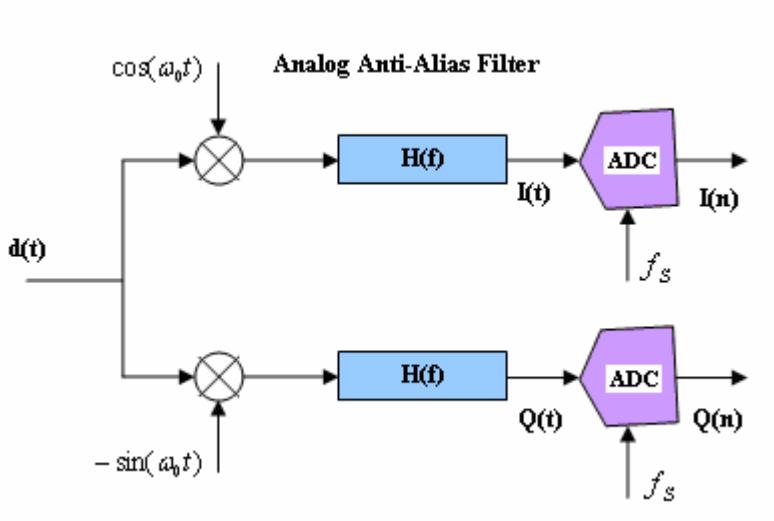


Traditional signal conditioning with analog anti-alias filter



DSP assisted signal conditioning with analog and digital anti-alias filters

Option-2



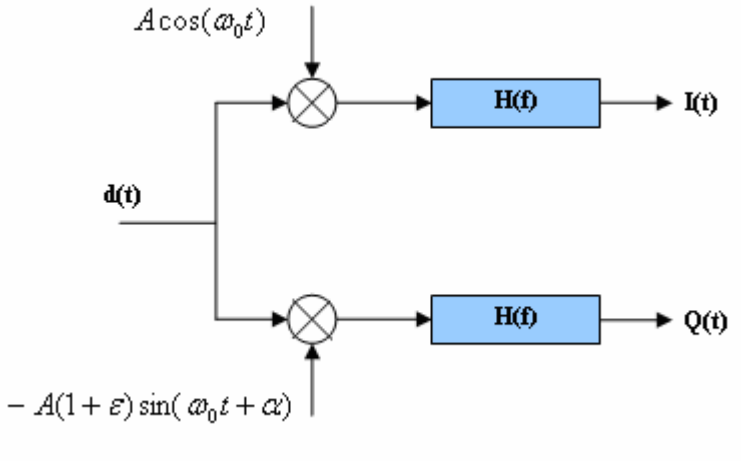
$$g(t) = A\{\cos(\omega_0 t) - (1+\varepsilon)\sin(\omega_0 t + \alpha)\}$$

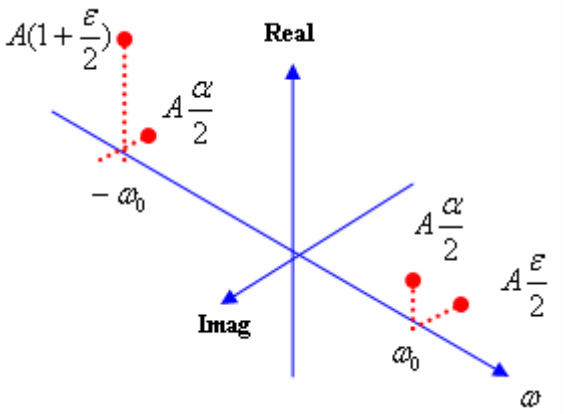
$$g(t) = \left\{\left[\frac{A}{2} - \frac{A}{2}(1+\varepsilon)\cos(\alpha)\right] - j\left[\frac{A}{2}(1+\varepsilon)\sin(\alpha)\right]\right\}\exp(j\omega_0 t) +$$

$$\left\{\left[\frac{A}{2} + \frac{A}{2}(1+\varepsilon)\cos(\alpha)\right] - j\left[\frac{A}{2}(1+\varepsilon)\sin(\alpha)\right]\right\}\exp(-j\omega_0 t)$$

$$g(t) \cong A\left[\frac{\varepsilon}{2} - j\frac{\alpha}{2}\right]\exp(j\omega_0 t) + A\left[(1+\frac{\varepsilon}{2}) - j\frac{\alpha}{2}\right]\exp(-j\omega_0 t)$$

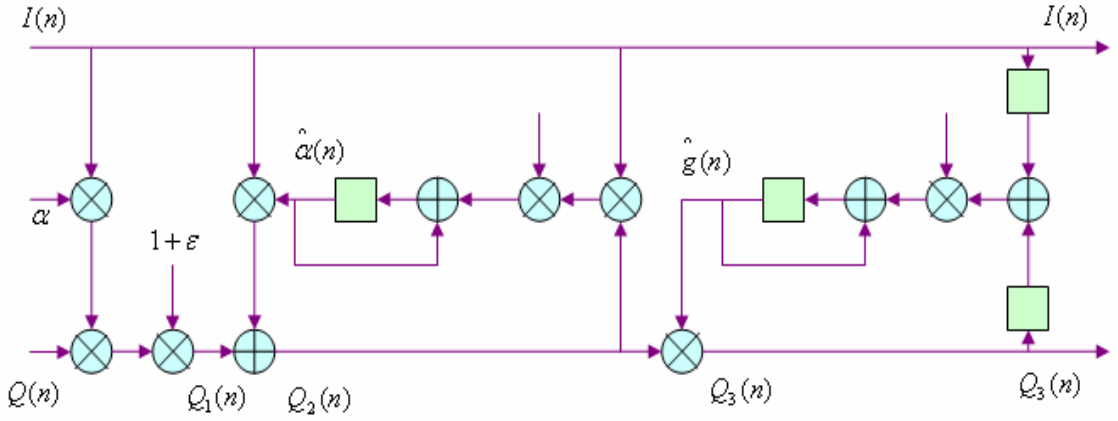
Traditional signal conditioning for quadrature down conversion





Spectral Components of unbalanced complex Sinusoid

Model of quadrature down conversion with gain and phase imbalance



Model of gain and phase mismatch in Quadrature Down Converter with block diagrams of algorithms that perform adaptive gain and phase balancing

$$Q_2(n) = (1+\varepsilon).Q_1(n)$$

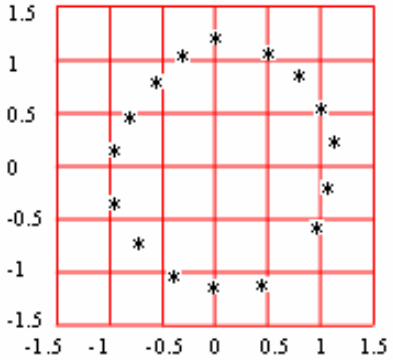
$$Q_3(n) = \hat{g}(n).Q_2(n)$$

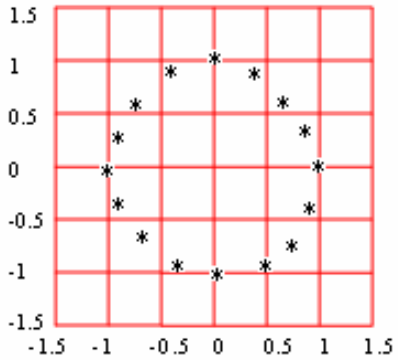
$$\hat{g}(n+1) = \hat{g}(n) + \mu\left[|I(n)| - |Q_3(n)|\right]$$

$$Q_2(n) = Q_1(n) + \alpha I(n)$$

$$Q_2(n) = Q_1(n) - \hat{\alpha} I(n)$$

$$\hat{\alpha}(n+1) = \hat{\alpha}(n) + \mu\left[I(n).Q_2(n)\right]$$





Constellation points from Quadrature Down Conversion with gain and phase mismatch before and after self compensating gain and phase balancing networks

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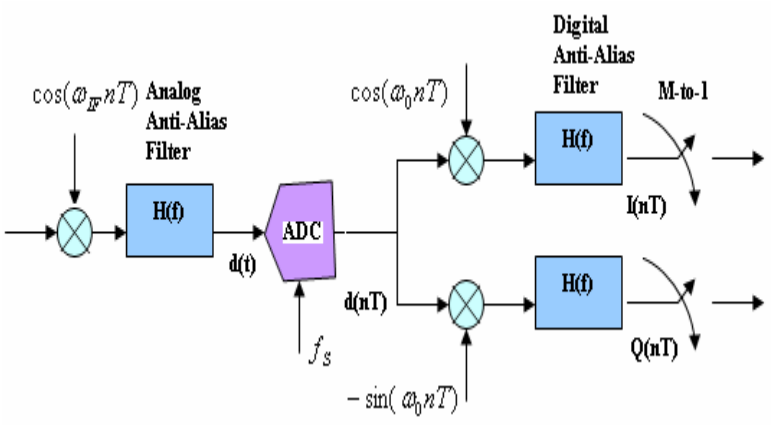
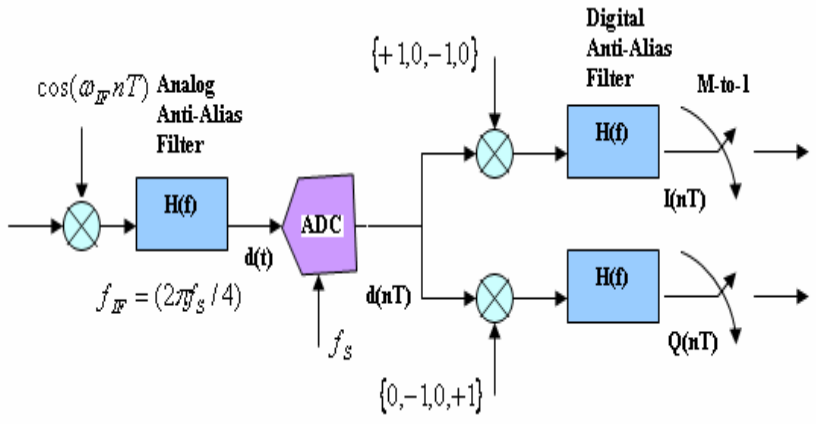
Option-3



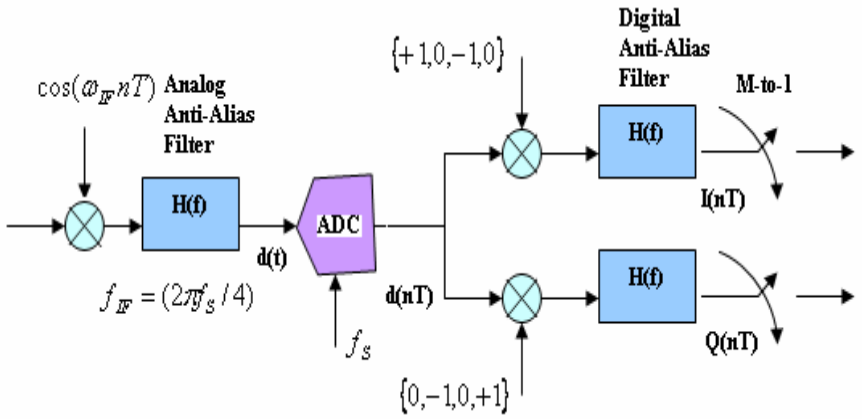
Block diagram of composite down conversion process: Sampling real IF signal followed by digital downconverter



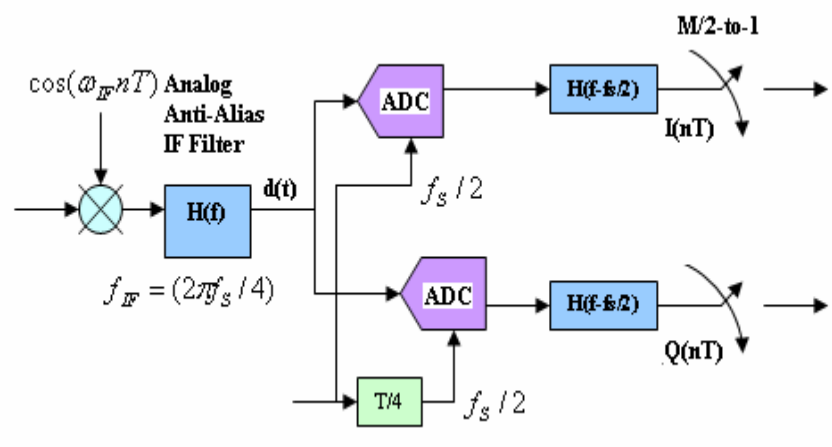
Block diagram of composite down conversion process: Sampling real signal on IF at quarter sample rate followed by trivial digital down converter with no multiplications

$$\omega_0 Tn\Big|_{\omega_0=\frac{2\pi f_s}{4}} = \frac{2\pi f_S T}{4}$$

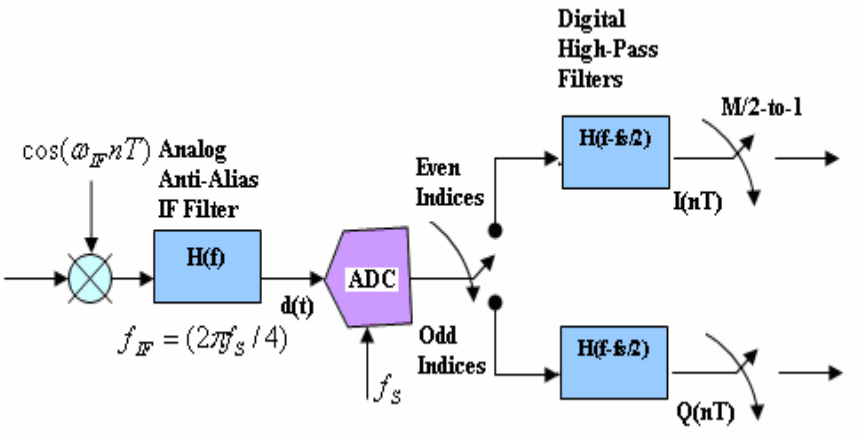
$$= \frac{2\pi(1/T)T}{4}n = \frac{\pi}{2}n$$



Block diagram of composite down conversion process: Sampling real signal on IF at quarter sample rate followed by trivial digital down converter with no multiplications



Block diagram of composite down conversion process: Sampling real signal on IF at quarter sample rate with two half rate, Offset T/4 ADC to form complex output stream



Block diagram of composite down conversion process: Sampling real signal on IF at quarter sample rate followed by commutator down sample and alias to half sample rate

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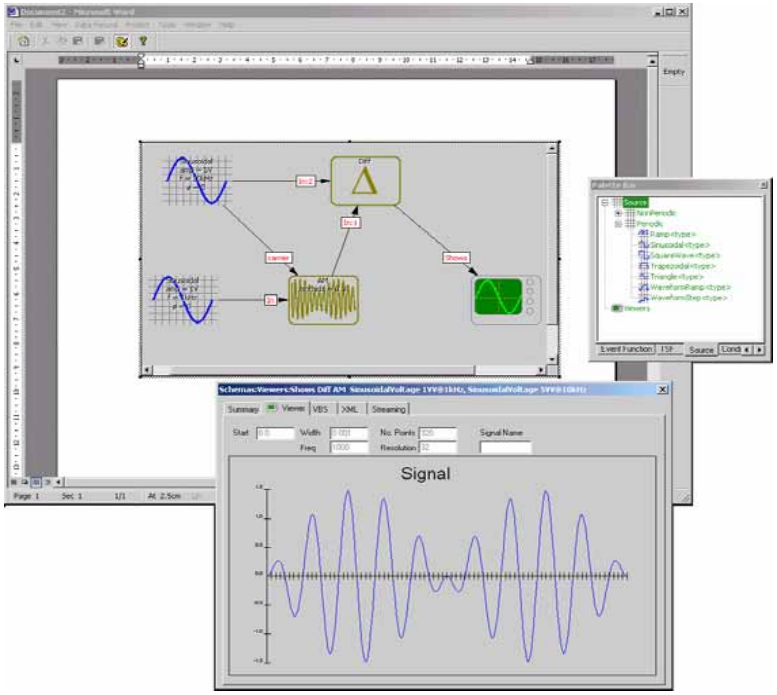
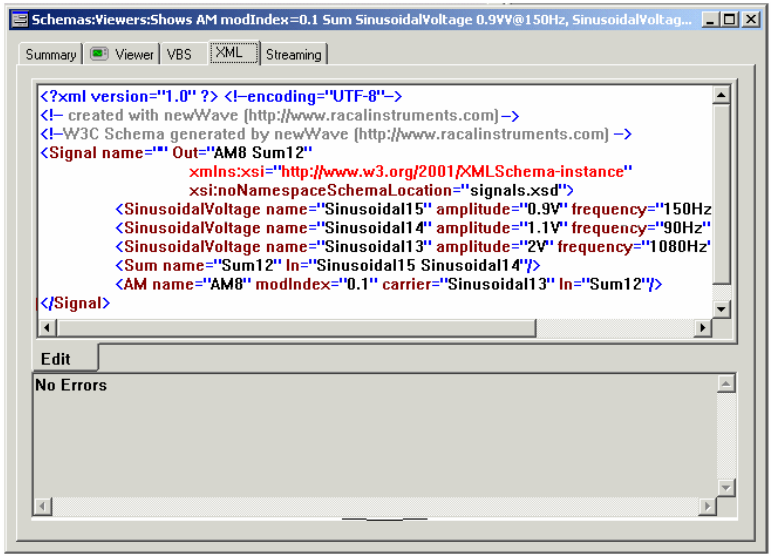
Signal and test description standard

- Modern PC
- Automated Test Program (ATP) design & Simulation
- Simulation
- ATE





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Real-World Examples

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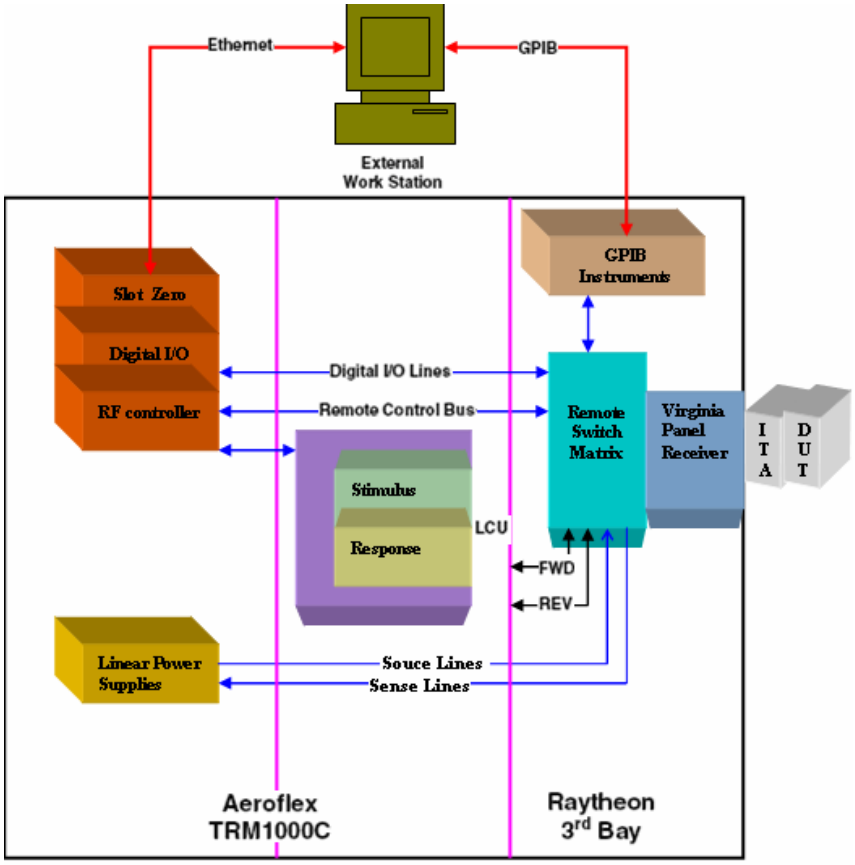
Universal high-speed RF Microwave test system



RFMTS Block Diagram

Logistical Goals

- Training for one system vs. many for operators, maintainers, and TPS developers.
- A modular architecture to facilitate: maintenance, fewer spares, and deal with obsolescence.
- A spares and maintenance program for one system
- A common resource that could be shared across many programs.
- An open architecture (H/W and S/W) that would permit upgrading / longevity.
- Reduced calibration equipment and procedures that employ automated / software based tools whenever possible to promote increased reliability and calibration integrity.
- System self test and diagnostic tools to support troubleshooting and maintenance.

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Parameters

Power	Isolation	Frequency
Tone Power	Conversion Gain	Spurii
Pulse Power (RMS or Peak)	Group Delay	Harmonic
Total Power	Noise Figure	Nth Order Intercept
Spectral Power Density	Phase Noise	Modulation Index
Noise Power	RF Signal Source	Raw Read
Pout & Pin at “N” dB compression	Complex Volts	Complex FFT Data Block
AM/PM	Pulse Profile	Digital Data Verification
Multiport S-Parameters	Rise time	Analog DMM
12-Term Error Correction	Fall time	Scope Measurements
Gain	Droop	Frequency
Input/Output Return Loss	Envelop Delay	Spurii

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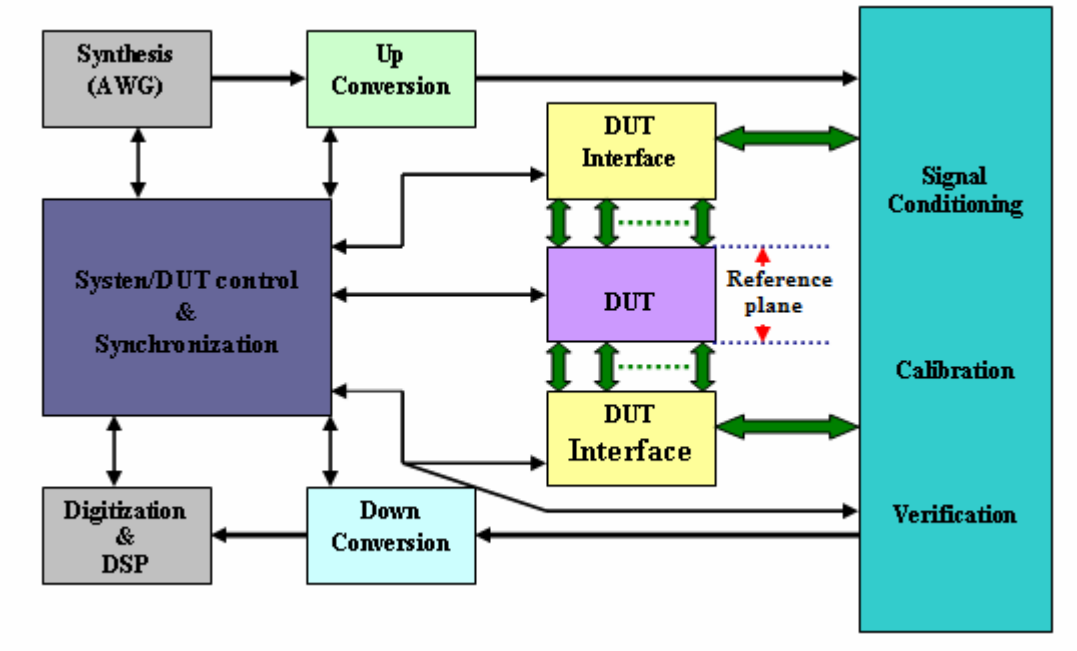

Microwave Synthetic Measurement Instrument Functional Diagram

Control and Data Acquisition

- Thirteen Slot VXI Chassis
- VXI Slot Zero Controller (COTS)
- VXI Digital Receiver (COTS)
- VXI RF Controller
- VXI Static Digital Card (COTS)
- VXI DUT Control Module
- Eight Port Ethernet HUB

Peripherals

- Host Computer
- Laser Printer
- Barcode Reader

Un-interruptible Power Supply

RF Subsystem

- Up-Converter & LO Distribution
- Down-Converter & LO Distribution
- System Local Oscillators
- 5 & 10 MHz Frequency Distribution Unit
- Optional Amplifier Bank
- RF Power Supply

Primary Calibrated Line Replaceable Units (LRU)

- Local Calibration Unit (LCU)
- GPIB Power Meter & Sensor (COTS)
- Noise Source (COTS)
- 3.5 mm Calibration Kit
- 3.5 mm plug/play THRU
- 10MHz Rubidium Standard

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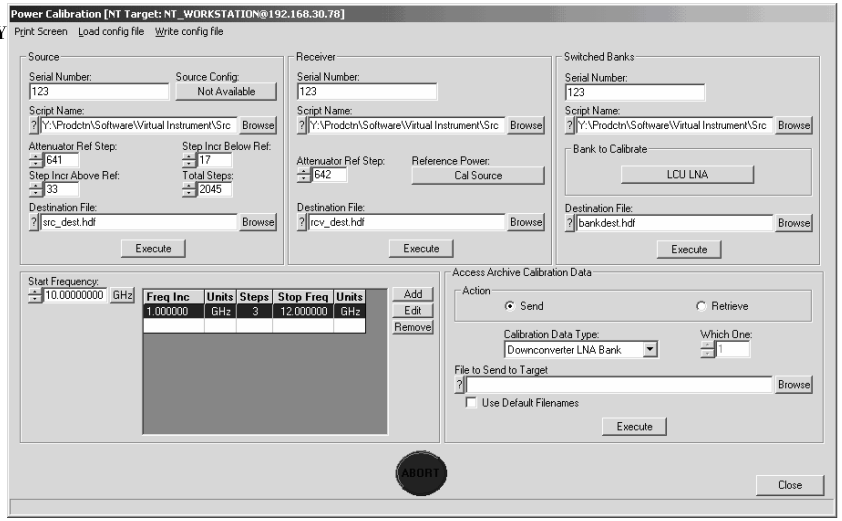
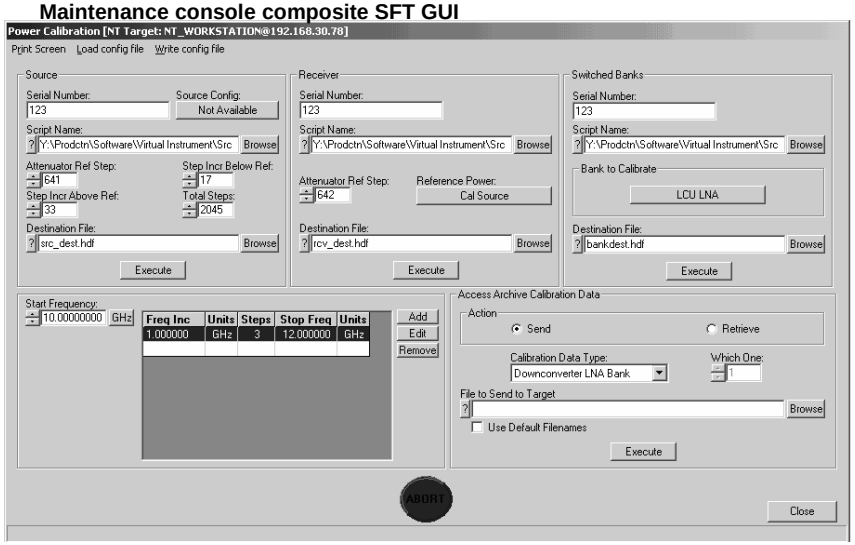
Maintenance console power calibration

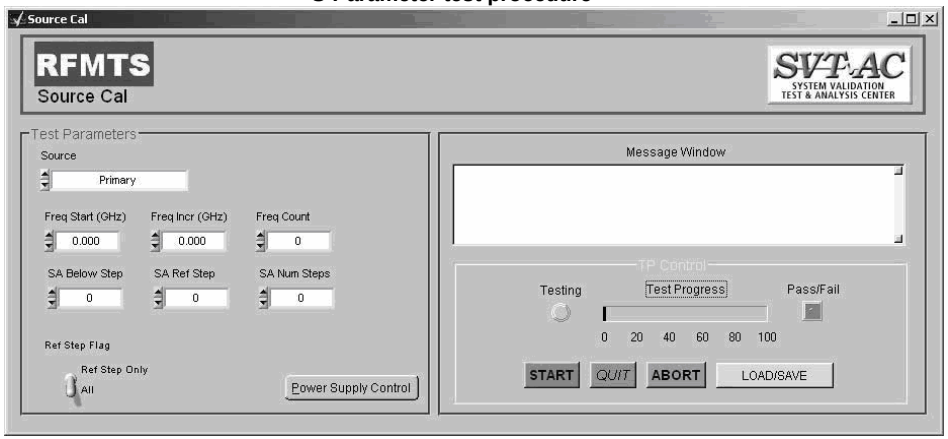


Maintenance console composite SFT GUI

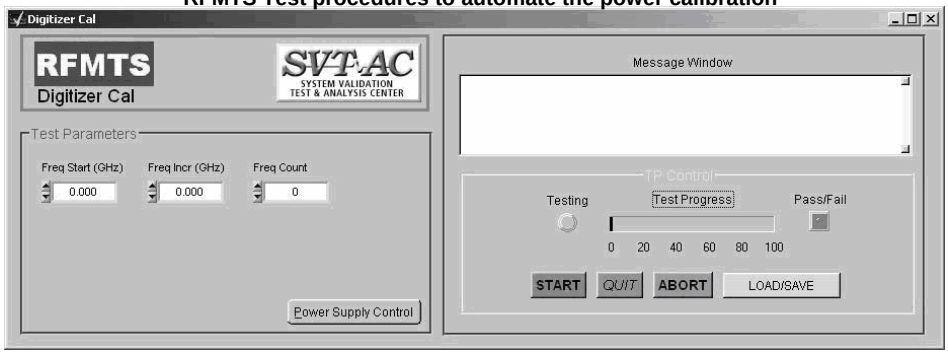


TRM 1000C maintenance console

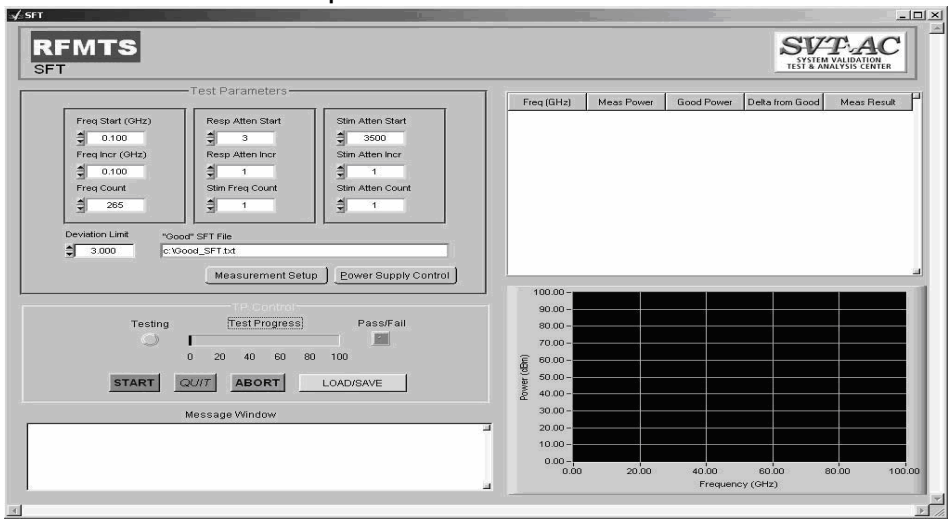
S-Parameter test procedure



RFMTS Test procedures to automate the power calibration



RFMTS Test procedures to automate the SFT



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Suggestions

Emerging systems will demand support for-

- Standards
- Mass Memory Tests
- New Busses
- Expanded frequency ranges
- Parallel processing/functional test
- Multiple runtime/operating environments
- High speed, high resolution ADC/DAC technology
- High resolution Reference Units

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Questions

Tack !