Boundary Scan DFT for Better Test Strategy

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KEYSIGHT TECHNOLOGIES

How good is my product?

What are the factors that influence test?

– Accuracy

– Yield

– Time-to-Market

– Optimizing Redundancies in Test Flow

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Is there a guiding principle to influence a good test?

A pre-determined and procedural approach to ‘Design For Test’

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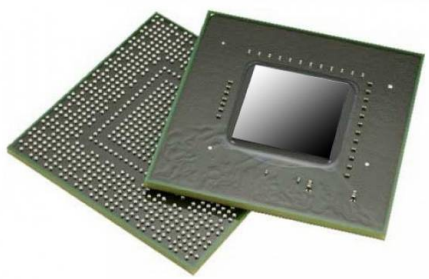
‘Design For Test’ or ‘DFT’

Concept that influences the design of a component or a system to facilitate in maximizing tests to diagnose structural defects

- Involves additional test circuitry added to designs
- Based on Boundary Scan Standard - IEEE 1149.1
- Test tools and methodologies maximizing defect detection

How Pervasive Is DFT?

- It is ALL PERVASIVE
- From Silicon all the way to System



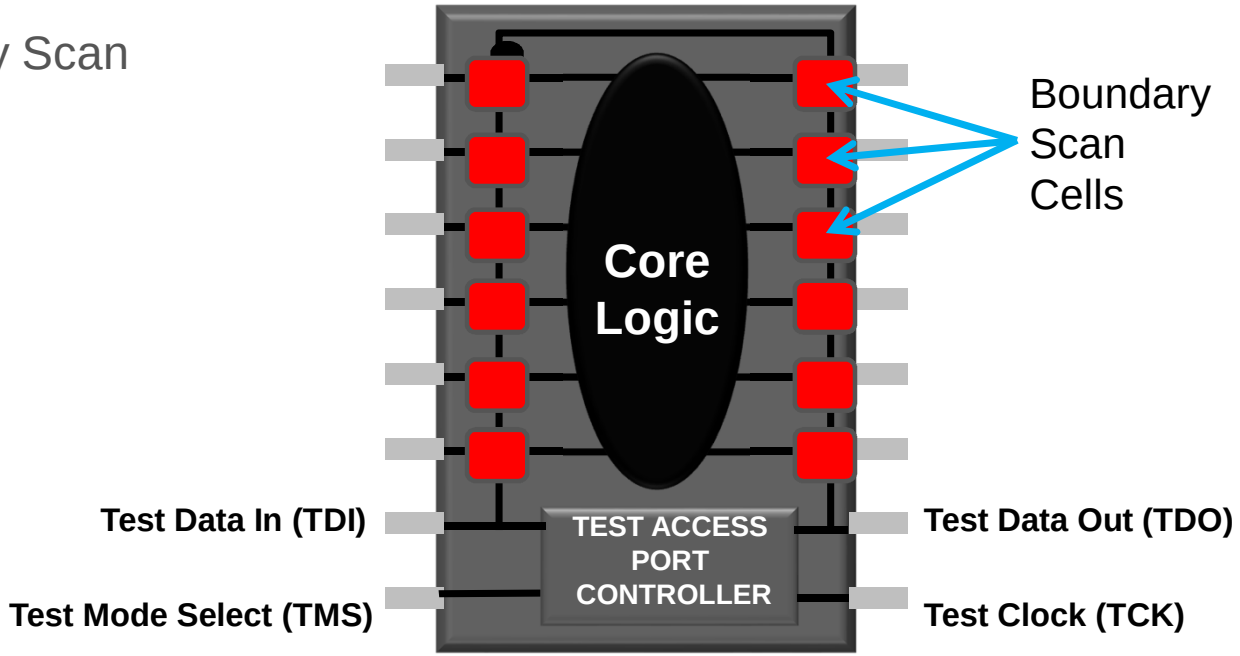
Chip Level DFT

Chip being the foundational block of a system, a well thought out DFT architecture always pays off for enabling determinism of quality

Many device vendors provide Boundary Scan enabled chips

DFT takes time and effort to implement

Well worth the effort as it impacts
chip to system level test quality



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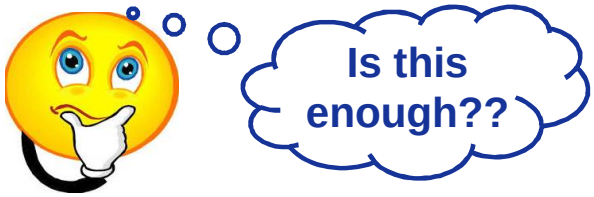
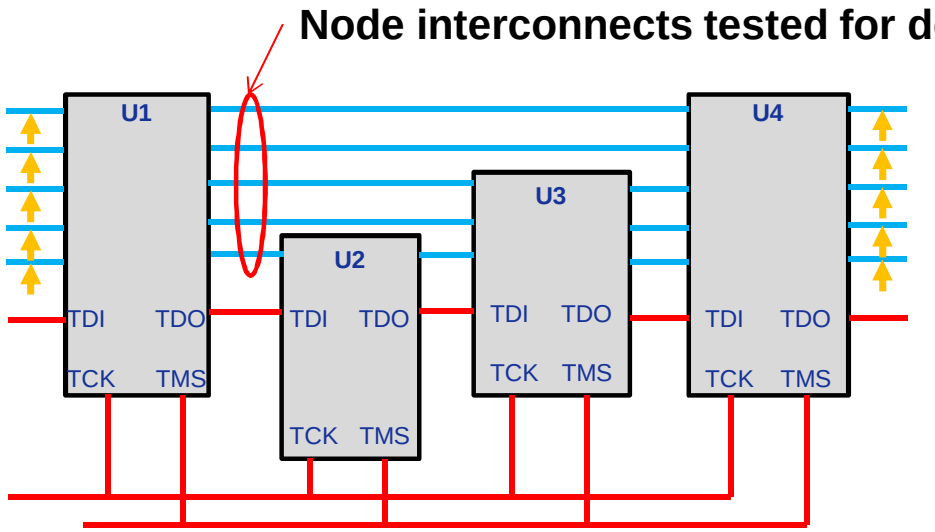
Chip Level DFT – Defect Detection Between Chips Enabled with IEEE 1149.x

With basic implementation of IEEE 1149.x enabled chips structural defects on boards arising on digital nodes interfacing with other chips can be detected



- Limits the defect detection to IOs on the chip
- Do all the chips have 100% BSCAN cells to its non power IOs?



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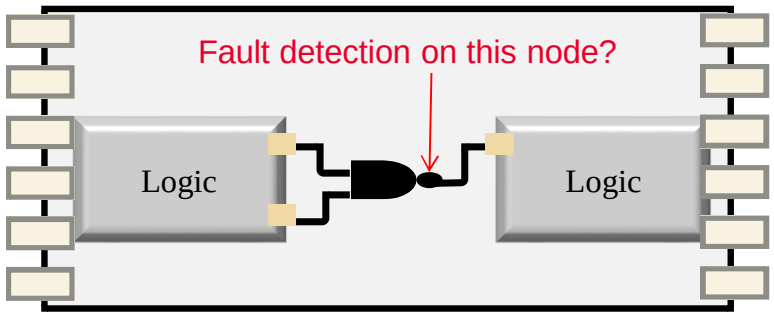
Chip Level DFT for Defect Detection In Logic

Basic implementation provides structural defect detection to IO interconnects between the chips

What about defect detection inside the chip?



I have Internal Scan!!!

🤔 Will it facilitate board level test?

Basic Boundary Scan cells can be leveraged to enable fault detection on the nodes inside the chips

How can this be facilitated?

- By enabling access to test structures inside the chip via BSCAN
- Enables testing at any level in the product flow – Chip, Board or System

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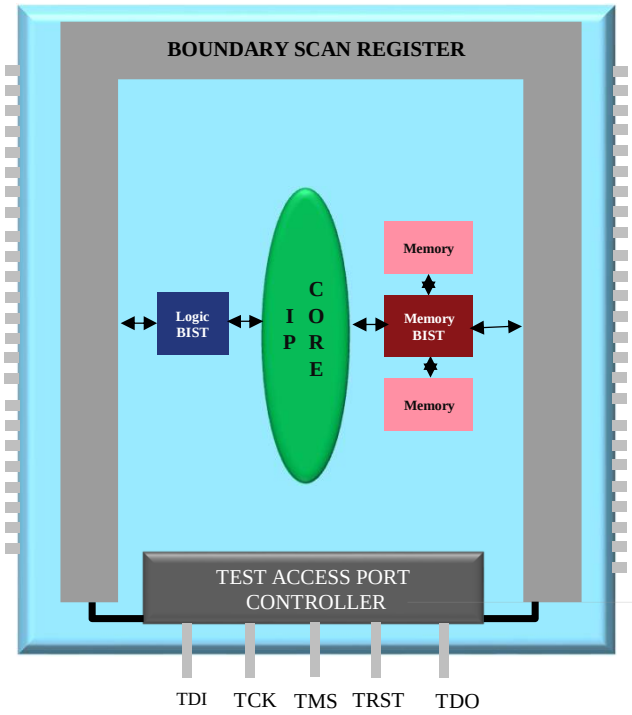
Chip Level DFT for Defect Detection - BIST



- Scan based test in the form of BIST (Built-In Self-Test) has made testing more effective and pervasive that can readily be used at any stage of the product life cycle – chip to system level
- BIST has made test generation and test application cost-effective. This has enabled increasing the test coverage of chips' internals.

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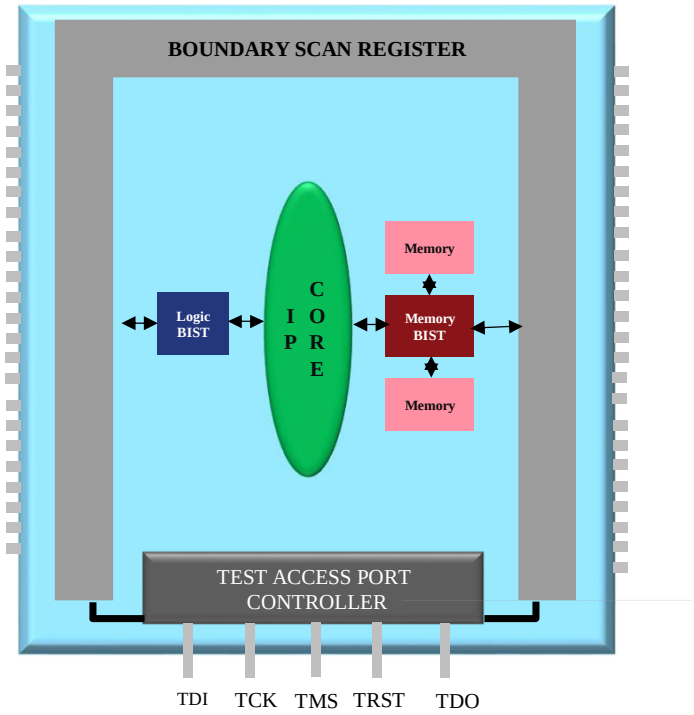
Chip Level DFT for Defect Detection - BIST



- Increase of System-On-Chip and System-In-Package designs necessitates an architecture for a flexible test methodology to be leveraged in multiple phases of the life cycle, ranging from chip test to system test
- Provides flexibility to test at different phases
- IPs can be re-used easily into different SOCs.
- Enabling a DFT scheme (BIST) on a chip accessible at system level will help in ensuring defect free systems
- New standards - IEEE 1687 and IEEE 1149.1-2013 cater to increasing the testability

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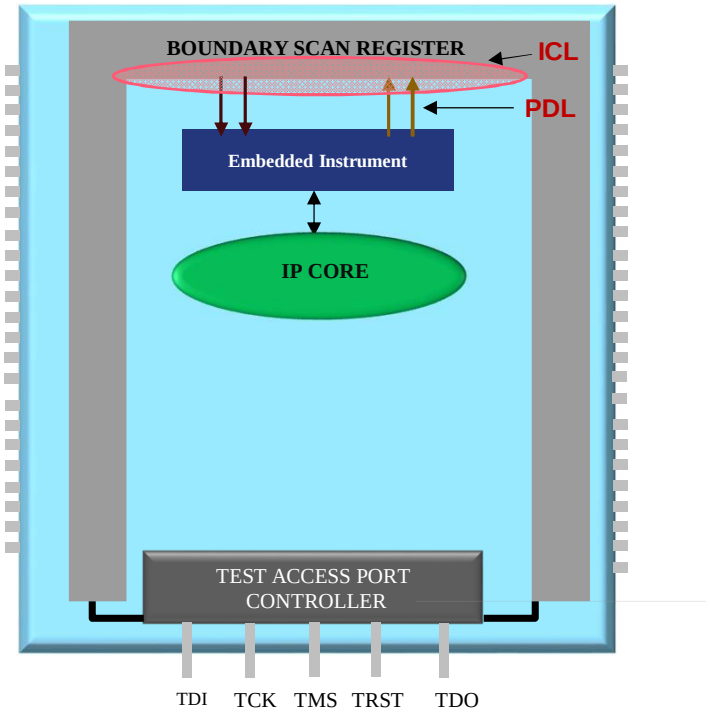
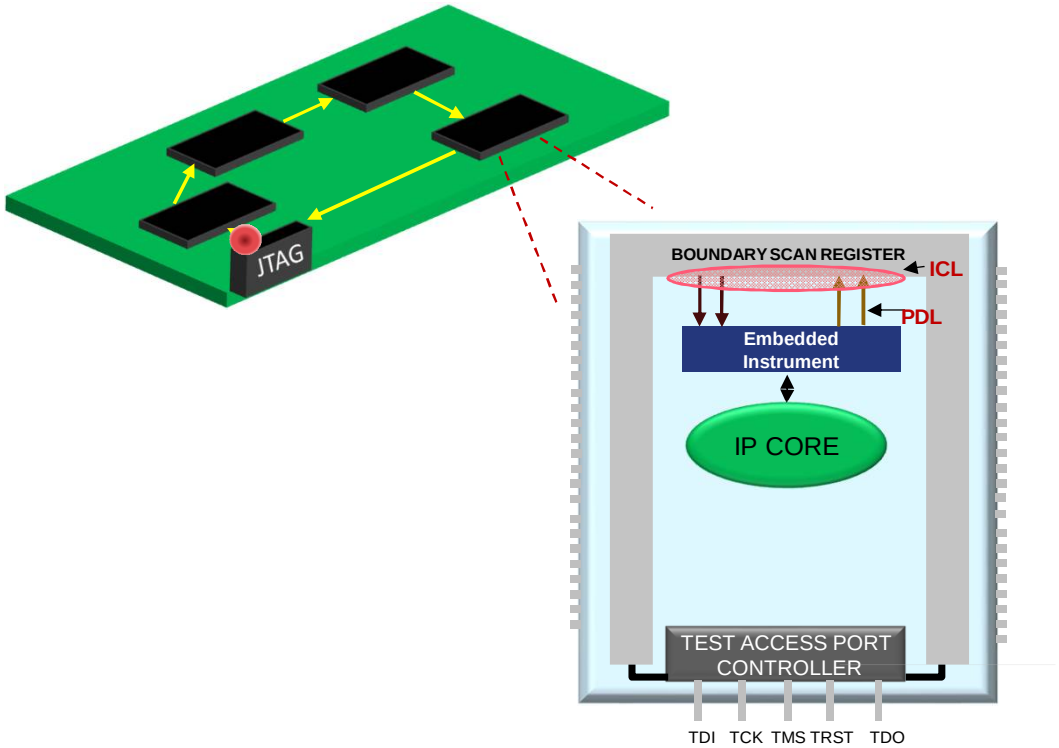
DFT Framework with IEEE 1687



- The DFT structures of the IPs are embedded as an instrument and 1687 describes the access to it via TAP using ICL(Instrument Connection Language) and PDL (Procedural Description Language).
- ICL describes the test access to the instrument and complete (or partial) connection networks.
- PDL facilitates test patterns retargeting to the 1687 instruments.

1687 Test Triggered at Board Level



Tests on the chip can be leveraged onto board level and turned on with board level structural test

Board Level Structural Test

Checks if the board is built correctly without any manufacturing or component defects

What are tested?

- Power
- Passive components
- BSCAN devices via BSCAN chain test
- Memories
- Connectors
- Non-BSCAN components via bed of nails

What tests are performed using BSCAN?

- Chain Integrity
- Validation of BSCAN cell access on each device inline with BSDL
- EXTEST for node interconnects
- Memories connected to BSCAN devices
- BIST
- Connector loopback

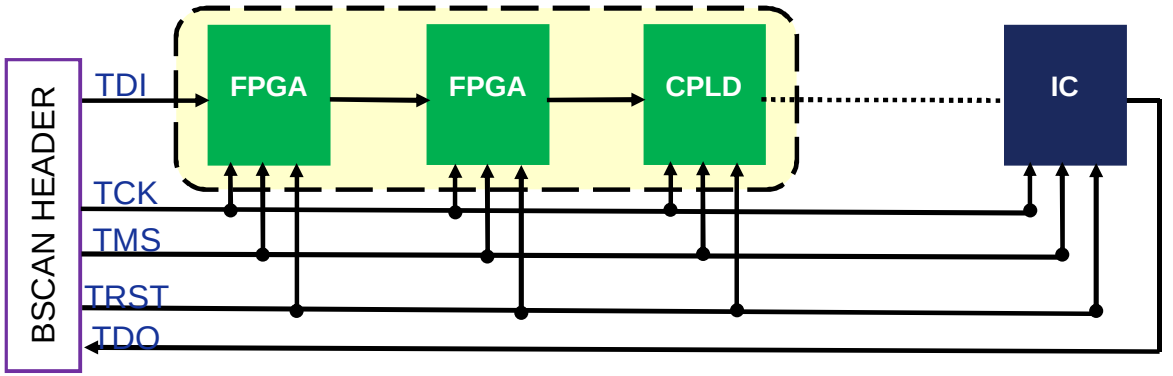
DFT investment ($$$ and time) pays off at chip and board test verification and production

What are the elements needed to ensure a good Board Level DFT?

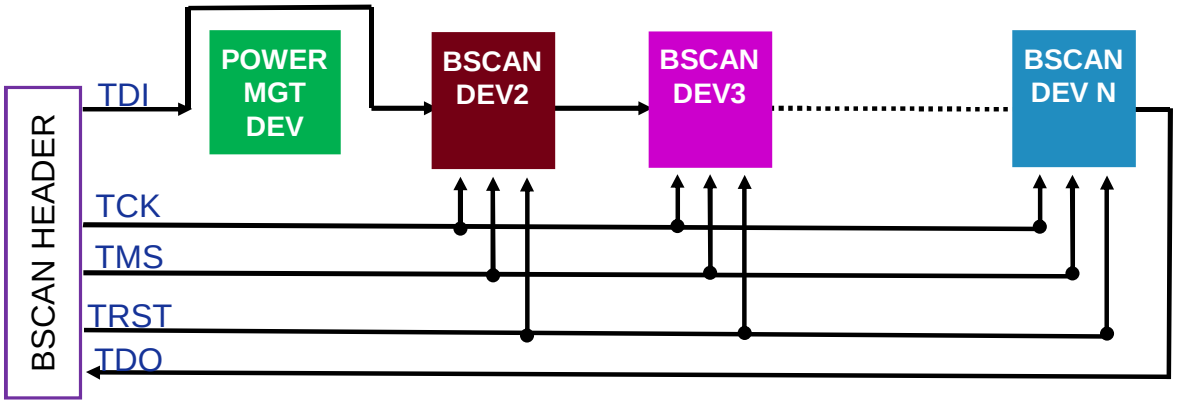
- First step is to choose IEEE 1149.X enabled device for the required functionality, if available.
- Design teams must qualify JTAG enabled parts to supplement into their functional requirements and specifications.
- Qualifying new devices compliant to IEEE 1149.1 standard by Procurement team facilitates an effective process for good DFT.
- Chain the devices with similar logic voltage together.

Board Level DFT Review – Good Practices

Boundary Scan Devices of similar logic are chained together.



Better to keep Power management ICs, out of the Boundary Scan chain as it may affect stability of the board during the test.



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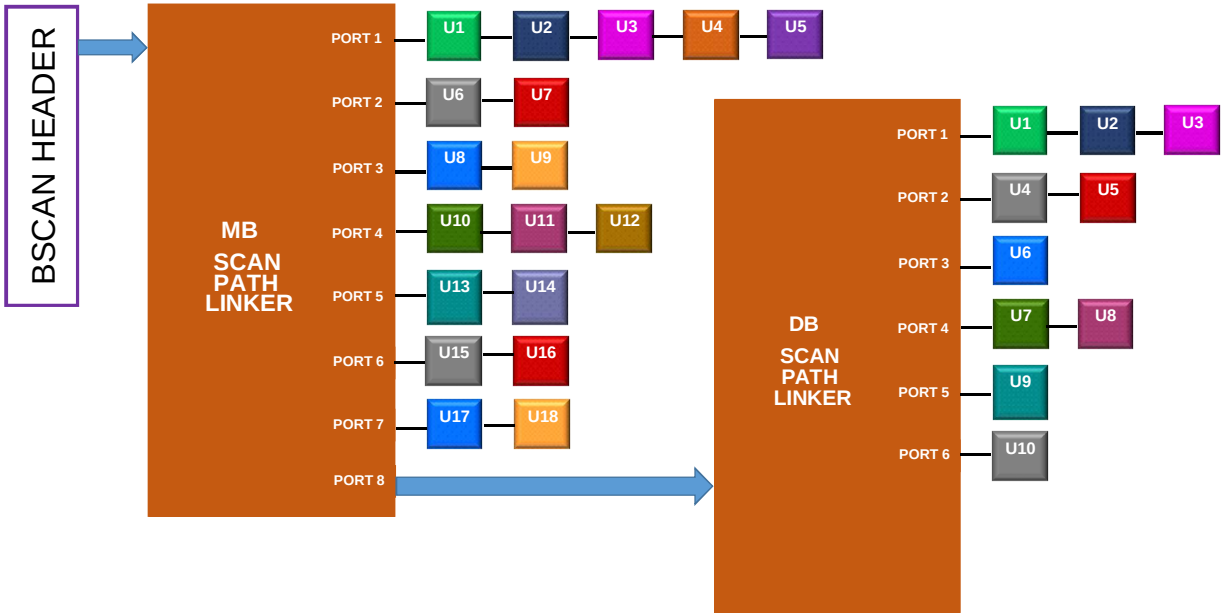
Board Level DFT Review – Good Practices

- On complex designs using a CPLD as a scan path linker, provides better management and flexibility of boundary scan chain in test.
- A scan path for each circuit (CPU block, Data Processing block, IO management, Memories, etc.) would help control the TAP signals independently.



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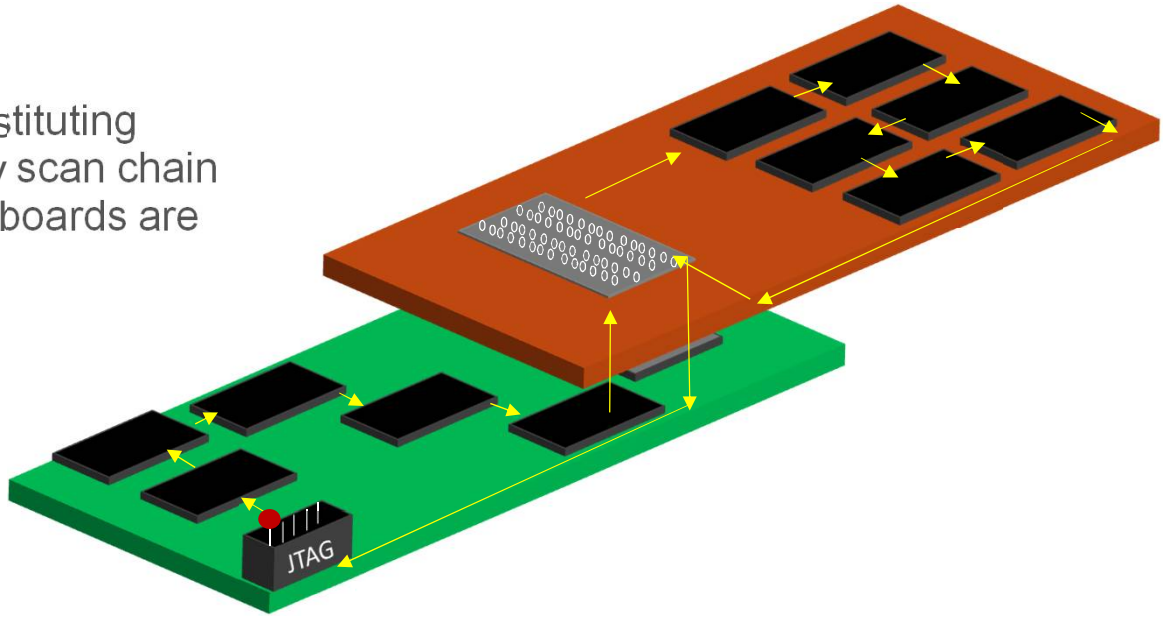
DFT on Multi-Board Configuration

- Effective system level DFT, involving multiple board configurations, making the boundary scan chain to be dynamically configurable in the system is of great value.
- Dynamic configuration of system constituting multiple boards enables the boundary scan chain to be tested as a system once all the boards are stacked.



Why?

- Detects any defects resulting from Board-to-Board connections
- It influences component reliability and yield traceability

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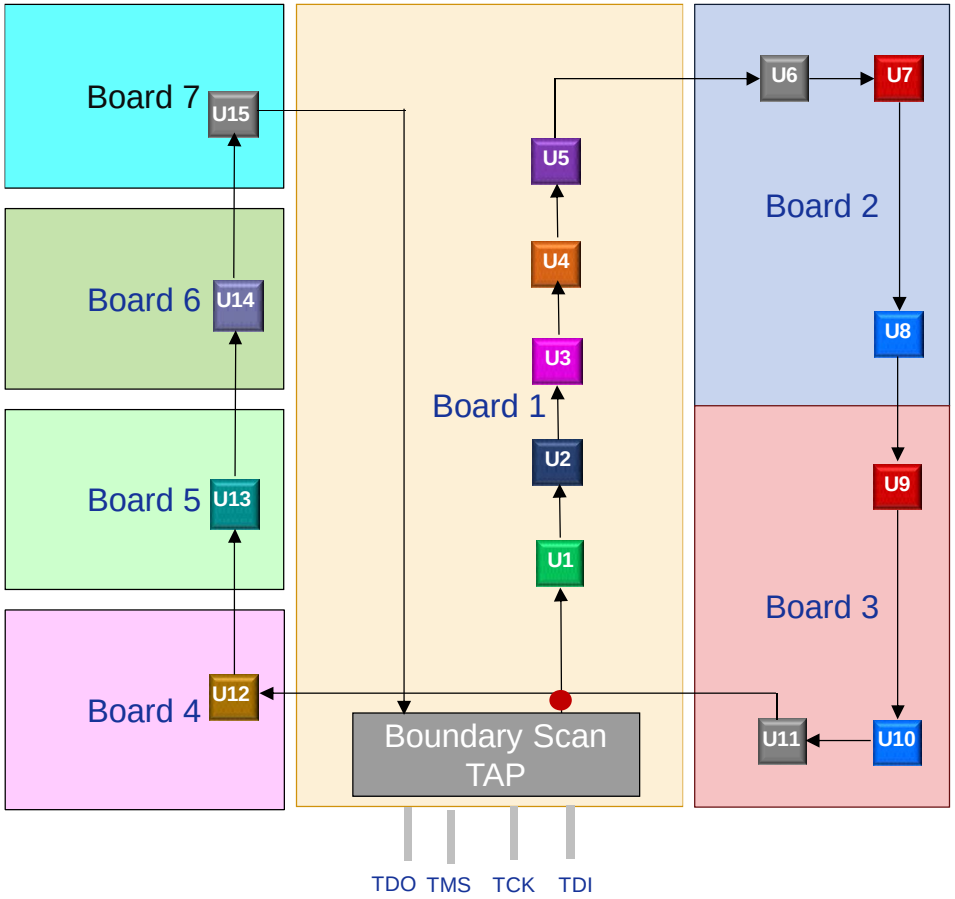
DFT on Multi-Board System Configuration

For multi board configuration programmable device provides options to run the tests in any phase of the product life cycle

- In Environmental Chamber test
- In the Field after deployment

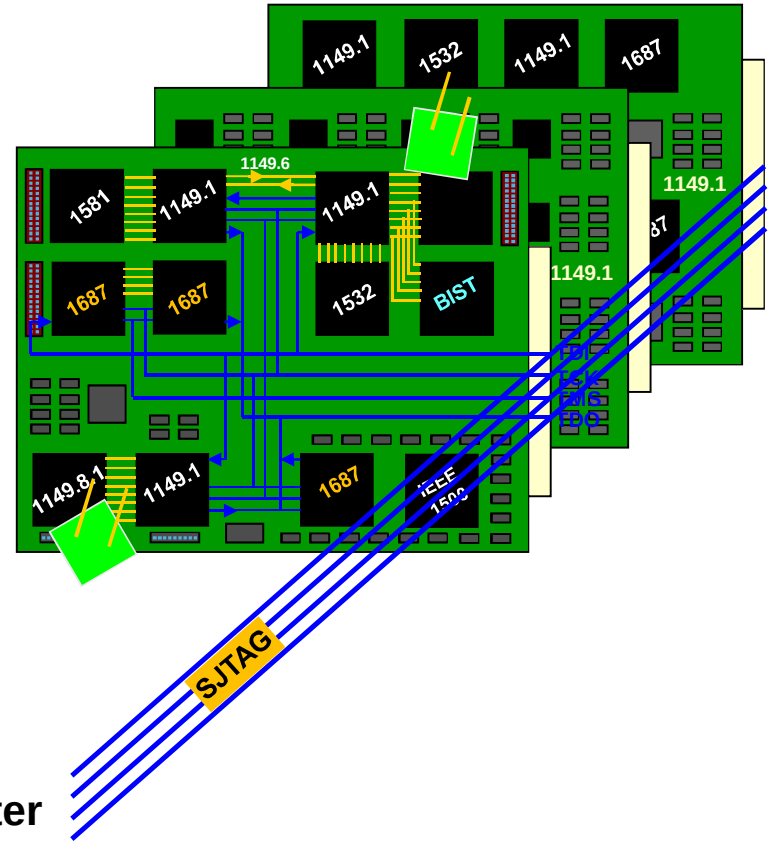
Why?

- Remote location testing
- Yield monitoring



IEEE Standards in Enhancing Boundary Scan DFT

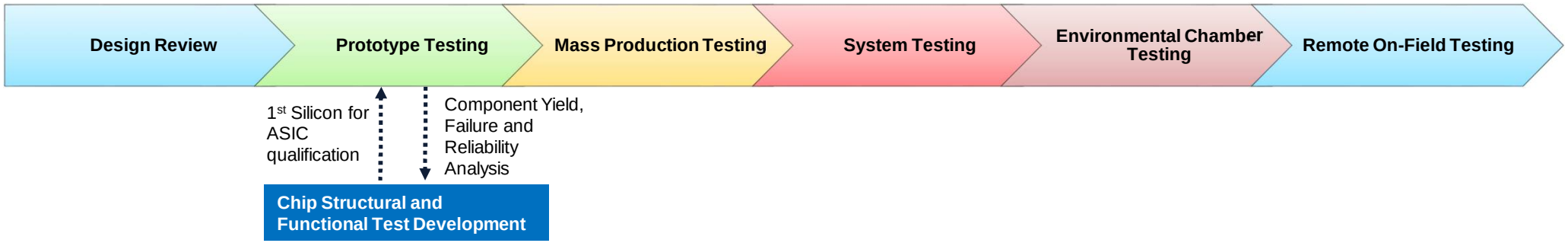
IEEE Std	Test Type	Application
1149.1-2013	Digital BSCAN	Connectivity (DC)
1532-2002	In-System Config	Device Programming
1149.6-2015	Advanced I/O	Connectivity (AC)
1500-2005	Embedded Core	Multi-core ASIC
1581	I/O loopback (w/o adding pins to device)	Non-BSCAN Memory Device (DDR, SRAM, FLASH)
1149.8.1	Analog-Dgital BSCAN	Connector & Non-BSCAN Device Powered OPENs
1687-2014	Internal JTAG	Embedded Instrumentation
SJTAG	System JTAG	System-based Connectivity (DC)
Proprietary BIST	Proprietary IJTAG	Embedded Test (IBIST)



Boundary Scan Board Tester
In-Circuit Testers (ICT)

Influence of DFT into Test Strategy

A good DFT from the chip level up to a system level, provides flexibility of testing the component and the system at any stage in the product life cycle.



- Review the design right at start with the first cut of files.
- Assess structural testability and BISTs for the ASICs.
- Enables in planning the functional test and mitigation for structural coverage loss.

- Turn on maximum testability during the proto phase.
- Validating good DFT in the Design Review will cater for more test coverage.
- This will mitigate the turning-on of functional tests until ready.
- Enable BIST tests to monitor the yield of ASICs and feedback the result metrics to the silicon team.

- Quick turn-on for Mass Production with updates to the Proto Test.
- If the yields from the BIST tests during Proto Phase is good, it can be turned off.

- Once individual boards are assembled into the system and before moving onto Functional tests, the system can be tested to ensure there are no handling defects introduced. Also, the aspect of low level diagnostics ensures saving root cause issues later in the Product Life Cycle.

- If the DFT enables on board programmable device capable of being the Boundary Scan Master, then, running the structural tests can verify how good the structural stability for varying environmental parameters are.

- Once the board is shipped, if the DFT has been enabled for triggering the test remotely (via on board diags with programmable device as the Boundary Scan master), any issues on the system can be diagnosed before making a call to RMA.

Conclusions

- **A good overall DFT enables identifying defects early in the process.**
- **A good DFT helps equip for comprehensive testability. This maximizes defect detection and in reducing NTF bone pile.**
- **The rework on the defects to fix happens in lesser events.**
- **All of these helps in reducing the scrap cost which will add back to savings as an ROI.**
- **RMA logistics costs will come down and increases reliability.**
- **Brand equity will rise.**

All of this starts with an early design review of the Boundary Scan circuit, during the design stage of board or system and, in maximizing capabilities of the DFT structures within chips.

Questions?