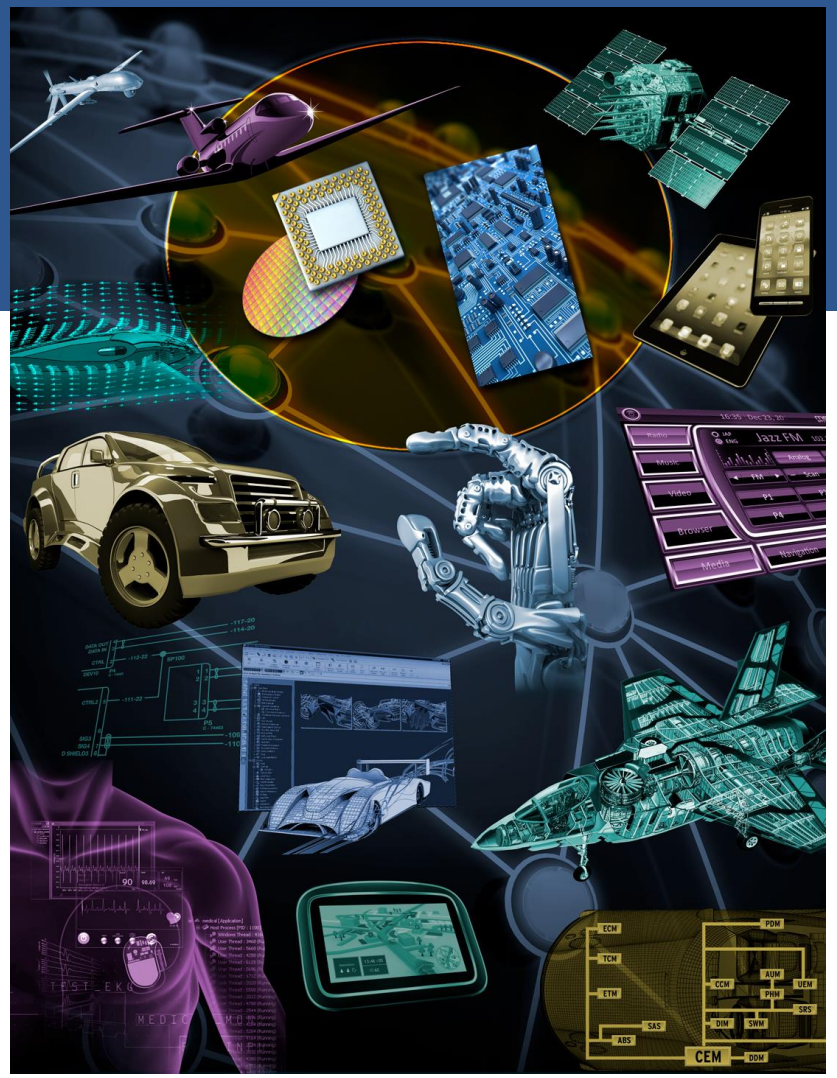

Improving Testability During PCB Design

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November 29, 2017

Nordic Test Forum

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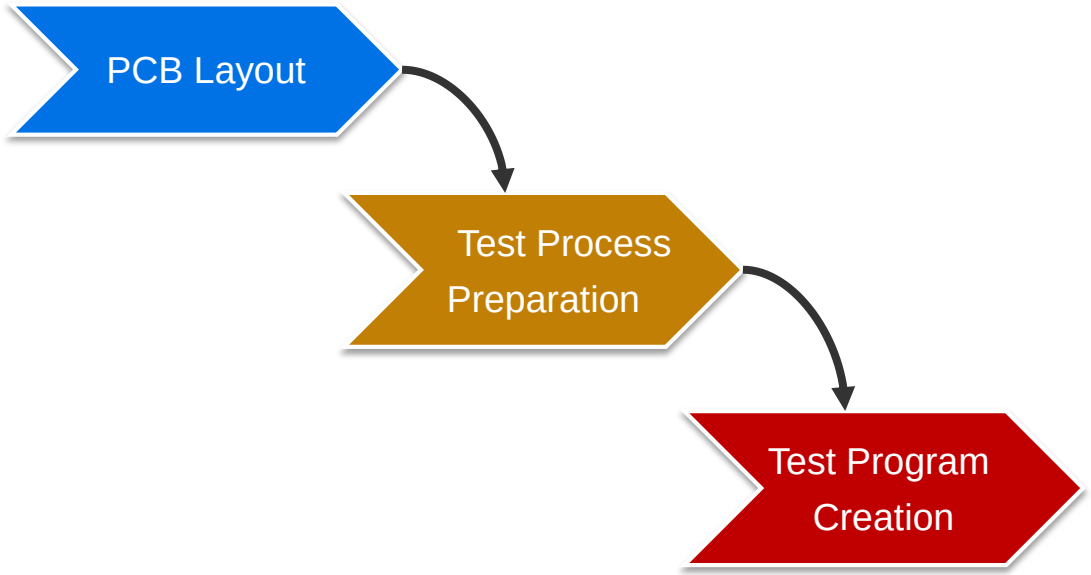
Typical DFT Design Flow Status



- DFT and testability analysis are after-thoughts
- Usually manual if at all
- Very reactive
- Input is received during later layout stages
- DFT input is low priority
- Whole DFT flow is fragmented
- Schematic is rarely considered

DFT Misstep: Transportation Industry OEM

- Phase 1 DFT considerations are scheduled for post placement
- Phase 2 are scheduled for post route
- Phase 3 are scheduled at sign-off

- If we get phase 3 done we are doing well

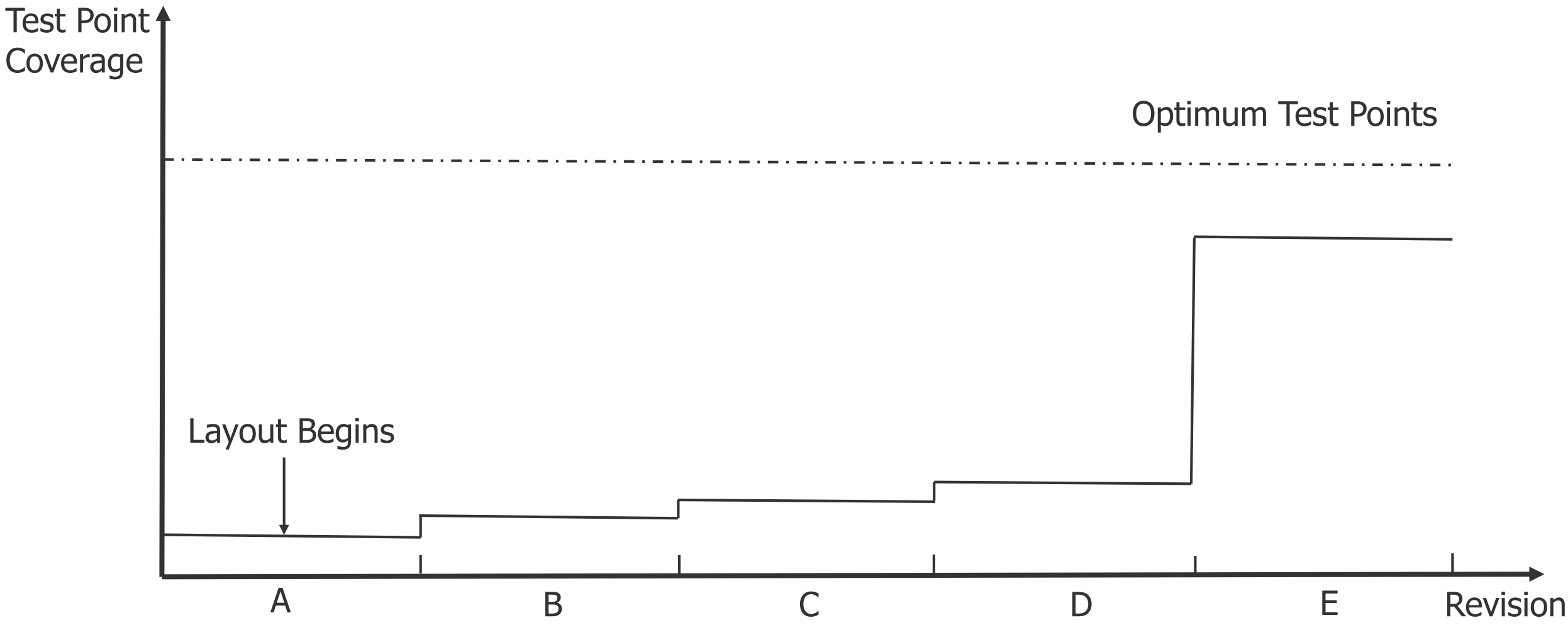
DFT Misstep: Boundary Scan Machine Vendor

- Boundary Scan vendor received an actual PCB
- Layout was completed and they were asked to show what they could do
- Vendor analyzed the design
- Handed it back saying “very little”
- Designers had wired the TCK and TMS pins on one of the boundary scan components incorrectly
- Nobody had noticed

DFT Misstep: Commercial OEM

- I was requesting feedback on testability coverage models
- Do you use any of the following:
  - "PCOLA-SOQ"?
  - "PPVS"?
  - "TPC"?
- Response from one OEM:
- If we could just understand if each component was tested or not we would be ahead of where we are today

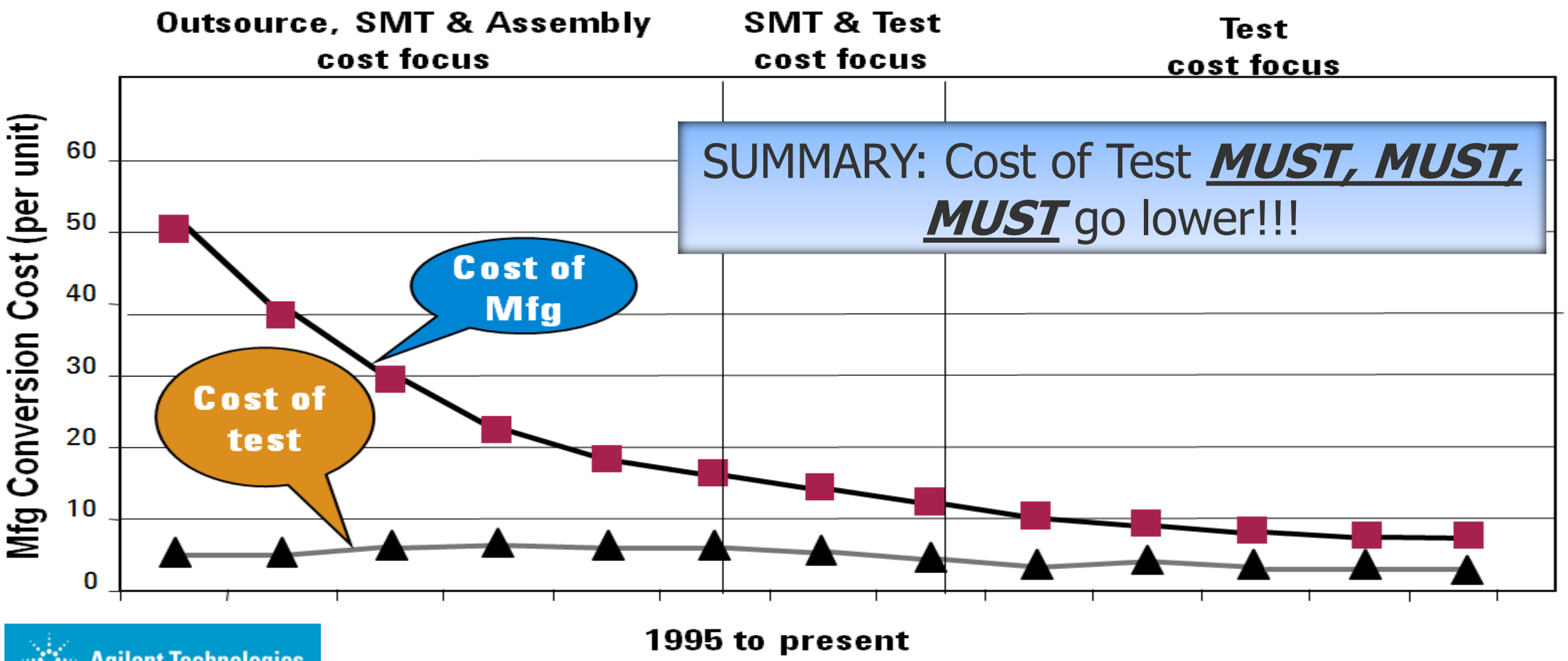
Existing Reactive Test Point Management



DFM Is Now A Proactive Step Of PCB Design

- DFM started as a post process of layout but is now left-shifted, concurrently with layout
- DFM has these benefits:
  - Reduces manufacturing issues
  - Increases yield
  - Reduces scrap
  - Simplifies rework
- So how has DFM best practices and lack of DFT best practices impacted overall electronics manufacturing?

Cost Of Test: The Final Frontier



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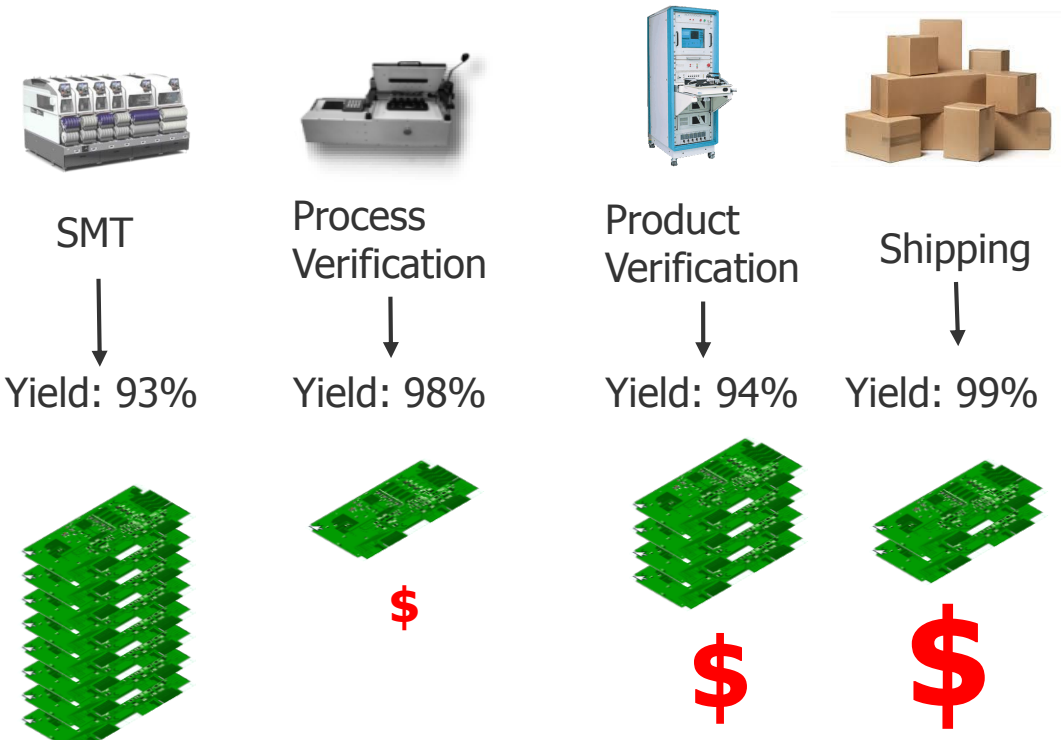
Consequence Of Using FT For Process Faults

- Defects will occur in manufacturing
- How will they be found?
- Poor coverage at process verification means high yield, but high escapes and hence lower yield at functional
- Cost of diagnosis and repair is higher at functional
- Increased opportunity for expensive field failures
- Boards scrapped, deliveries slipped, revenue targets missed



External Industry Factors

- High volume production still mostly done in China and PacRim
- Seeing increased manufacturing in Americas, Europe and Japan
  - Higher mixes, higher variants, lower batch volumes
  - More and more products being designed
  - Shortening the time to market in the NPI phase
- Fewer test engineers coming in to the industry
- Manufacturing engineers wearing more hats
  - Process engineers taking on test engineering responsibilities
- Design engineers wearing more hats

A Look Into The Future

- Current environment is not sustainable
- Number of test engineers cannot keep up with the number of products being produced
- Defects will continue to occur in a high mix, lower volume environment
- Existing reactive DFT environment must change
- DFT and testability analysis must become proactive
  - DFT must repeat the usage and acceptance of left-shift DFM

Opportunities For Being Proactive

- Considering test analysis at layout is too late
  - Too many decisions have been taken already
  - Limited opportunity to affect change without causing knock-on effect
  - Layout will naturally be sub-optimum for test purposes
- Input must begin with schematic analysis
- Must consider DFT input as any design constraint
  - Just like other design constraints
  - Mechanical, electrical, signal integrity, power integrity, etc

Test Point Placement Challenges

- CAD layout tools have great solutions to place test points
- Most designs do not have the space to place test points on all nets
- Need to know which nets need test points and which do not
- Must know this before layout is started
  - Test point requirements need to be a constraint
  - Test points need to be considered with the other design constraints
  - Leaving this to later in the layout phase is too late
  - Most decisions have already been made, cost of change is too great
- Test point requirements must be proactive, not reactive
- How do we know which nets need test points and which do not?

What If We Cannot Achieve 100% Access?

- Even with 100% access, we cannot achieve 100% coverage
- What happens if I can't get 100% access?
  - Insufficient PCB real estate
  - Sensitive signals, can't tolerate load of a test point
- PCB layout will add test points where they can
- PCB layout will not place test points where it can't
- But surely that will result in a sub-optimal layout for test?
- So we need to get proactive and request test points where we need it
- Let's review some techniques that can help overcome lack of access

Need For Proactive Test Point Management

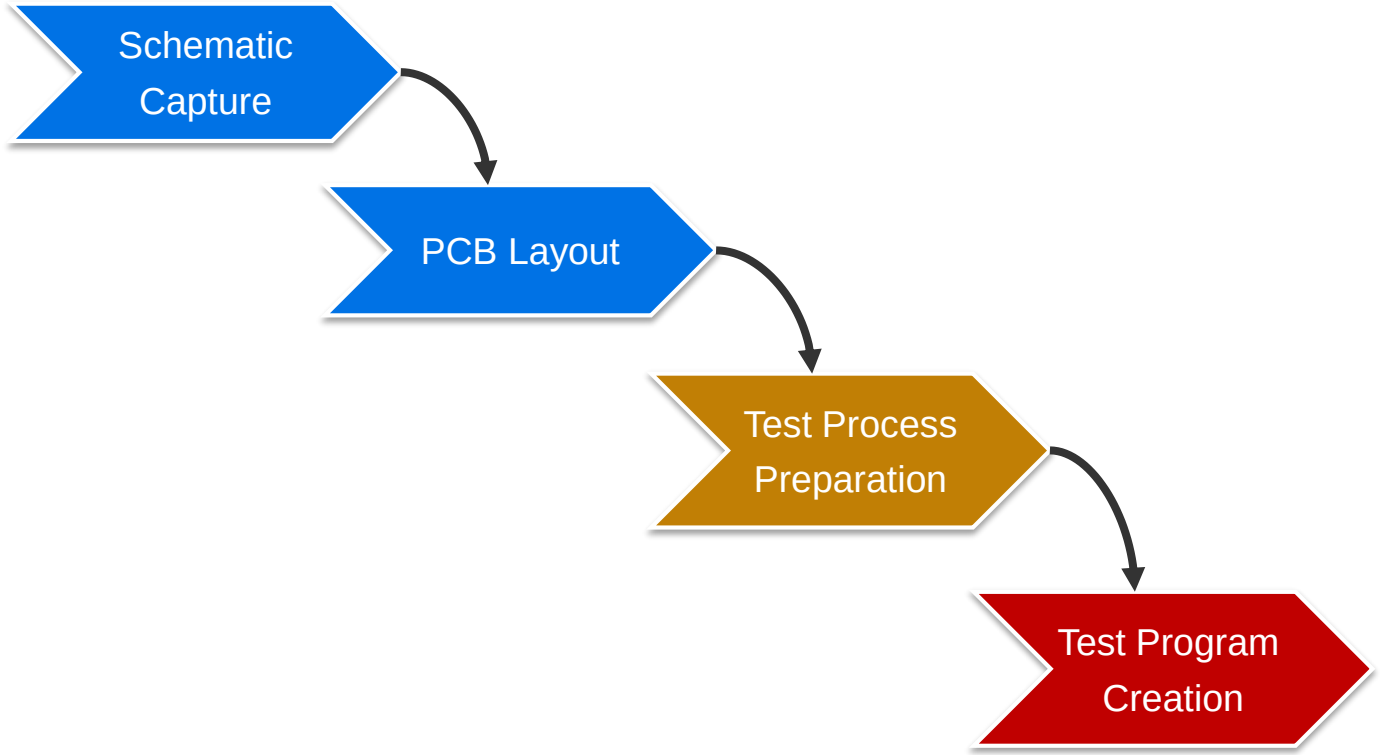
- Opportunities for removing test points
  - Boundary scan nets
  - Series resistors
- Low value resistors
  - Need additional test points either side of the component
  - 2 test points each for a total of 4
  - Allows effect of the resistance in fixture wiring to be eliminated
  - Typically limit is around 50ohm
    - Resistors above this limit can usually be tested with single test point on each side
- Power injection
  - For powered up test, need test points to inject power on to the board
  - Can be 10 to 20 test points per power rail net
  - Can be based on the current requirements of the design

Overall Results Of Proactive Test Point Analysis

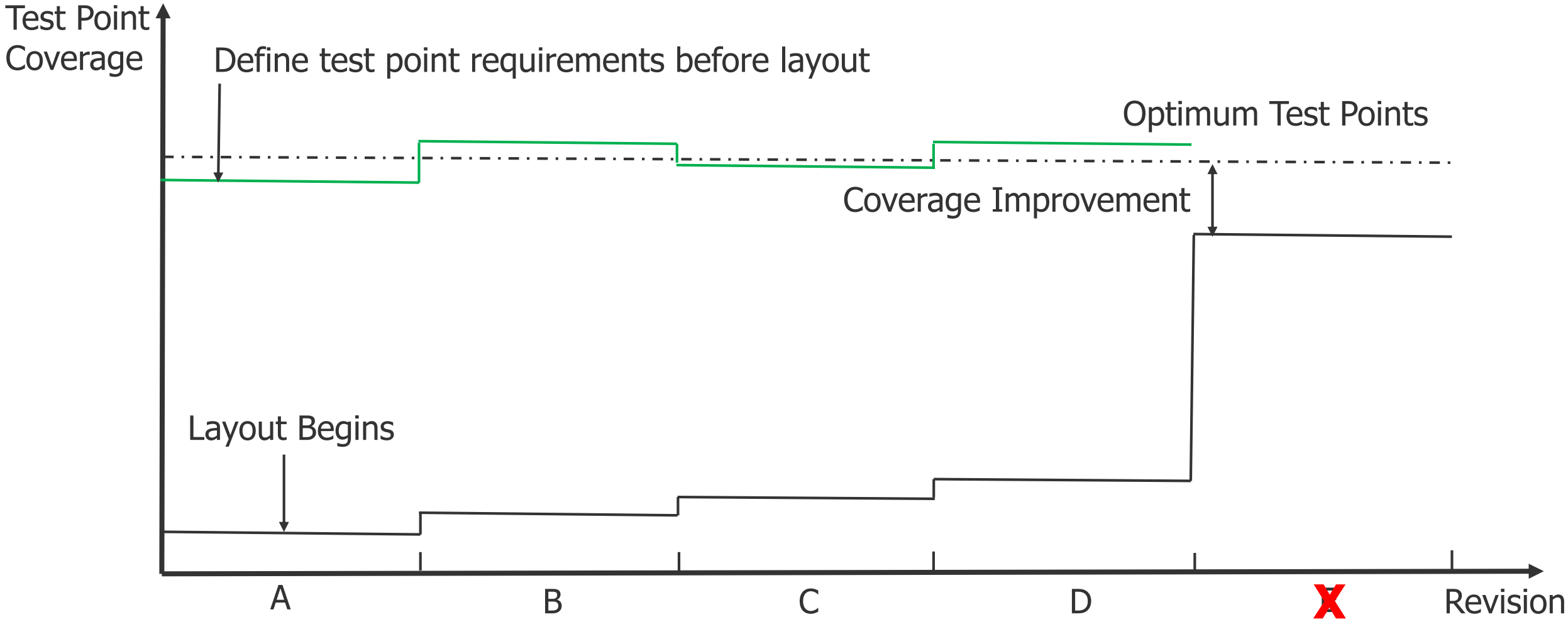
- Many techniques to reduce test point requirements, without compromising test coverage
- All these techniques can be used to reduce test point requirements across a design
- It is component and design dependent
- It may not be possible to get everything test needs
- But it is better to be mostly proactive as opposed to completely random
- Maybe further negotiation is possible to improve the initial DFT implementation

Optimum DFT Design Flow

- DFT and testability start at schematic capture
- Test point requirements are an input to layout
- Testability is further managed during layout
  - What is requested may not be possible
- DFT Design flow becomes proactive

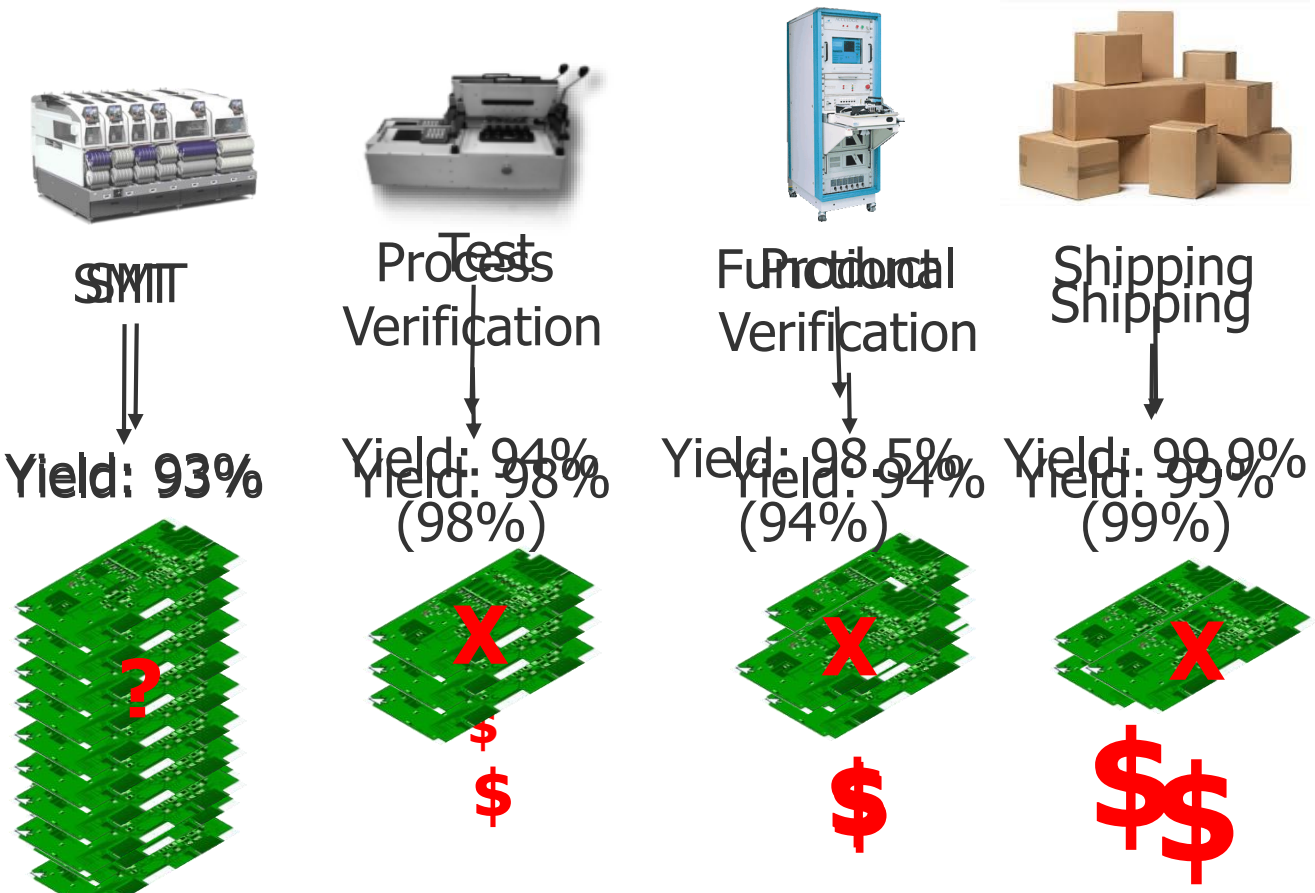


Future Proactive Test Point Management



Benefits Of Proactive DFT In The Design Flow

- Here's the picture from before
- But with a proactive DFT strategy
- SMT defect rate is the same
- Yield is lower at Test
  - But much higher at functional
  - Failing boards are fixed faster
  - Less likely boards are scrapped
- Savings are significant when building in hundreds, thousands or millions of boards



Summary

- Testability considerations must be proactive
  - A reactive test strategy is not sustainable in today's high mix environment
- Testability must start from the schematic stage
  - Leaving DFT until layout guarantees a suboptimal product quality
- Let's have DFT repeat the success of concurrent DFM but in a shorter timeframe

- Any questions?

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