The Odds of Test and Measurement

Hans Manhaeve
Ridgetop Europe

Setting the Scene

- Electronic System :
  - "Assembly of the individual components and the interconnection between these components"
- Components:
  - Each component may consist of sub-components and interconnects

?? How do we test and qualify interconnects ??

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Challenges

- Interconnect quality and reliability assurance
  - 2.5/3D integration
  - Package qualifications
  - Device to board
  - Wires & cables
- Die crack detection
- Contact quality
  - Degraded – intermittent – permanent failure
- Life-time monitoring

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect Failure

- Interconnects are subject to
  - Manufacturing defects
  - Aging effects (electromigration)
  - Stress (thermal, electrical, chemical, mechanical, vibration)
- Detection can be
  - Easy – opens/shorts
  - Cumbersome – degradation/intermittencies

NTF Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect Integrity

- Validating whether the connection is good or bad
- Good Connection:
  - Low resistance (typ. < 1 Ω)
  - No Disruption on data
- Bad Connection:
  - From resistive to Open – very high resistance (typ. > 1MΩ)
  - Short
    - → Short to ground (stuck-at 0 - s@0)
    - → Short to supply (stuck-at 1 – S@1)
    - → Short to other signal line
  - Intermittent
    - → Temporarily open
    - → Temporarily short

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect Reliability

- Validating whether the connection *remains* good over time
  - Check for degradation
  - Check for intermittencies
- Requires observation over time
  - Continuous observation
  - Observation at discrete time points.

NORDIC TEST FORUM

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Intermittent Faults

- According to Standards:
  - An interconnect intermittent fault is an event that causes the interconnect resistance to increase for a predefined amount and last for a minimum time.
  - Fault detection is linked to # of occurences
  - Definition evolved:
    - → From: R increase of 1KΩ lasting at least 1µs
      - JEDEC 22-B111
    - → To: R increase of 200Ω lasting at least 200ns
  - Interconnect is classified as failing if subsequent to the occurence of the first event, nine more events are detected that occur within a period of time T2 that is less than or equal to 10% of the time to the occurance of the first event T1. $(T2 <= 0.1*T1)$
- Reality
  - A single intermittence can cause a system to fail
  - NTF/NFF – RTOK – CND issues

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect Verification Techniques

- X-Ray Laminography
- Analog Harmonic Test
- RF induction & Analog junction technique
- Boundary Scan
- Daisy chain of interconnects
  - Qualification only

- ***SJ BIST***

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

What is SJ BIST?

- SJ BIST = Solder Joint Built-in Self-Test
  - "Solder Joint"
    - Interconnection between Device & Board
    - Can be seen as reference to *any type of connection*
    - Originally developed for FPGA-BGA applications
  - "Built-in"
    - Part of a "host" circuit
  - "Self-Test"
    - Host circuit can test itself.

NTF Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

What is SJ-BIST?

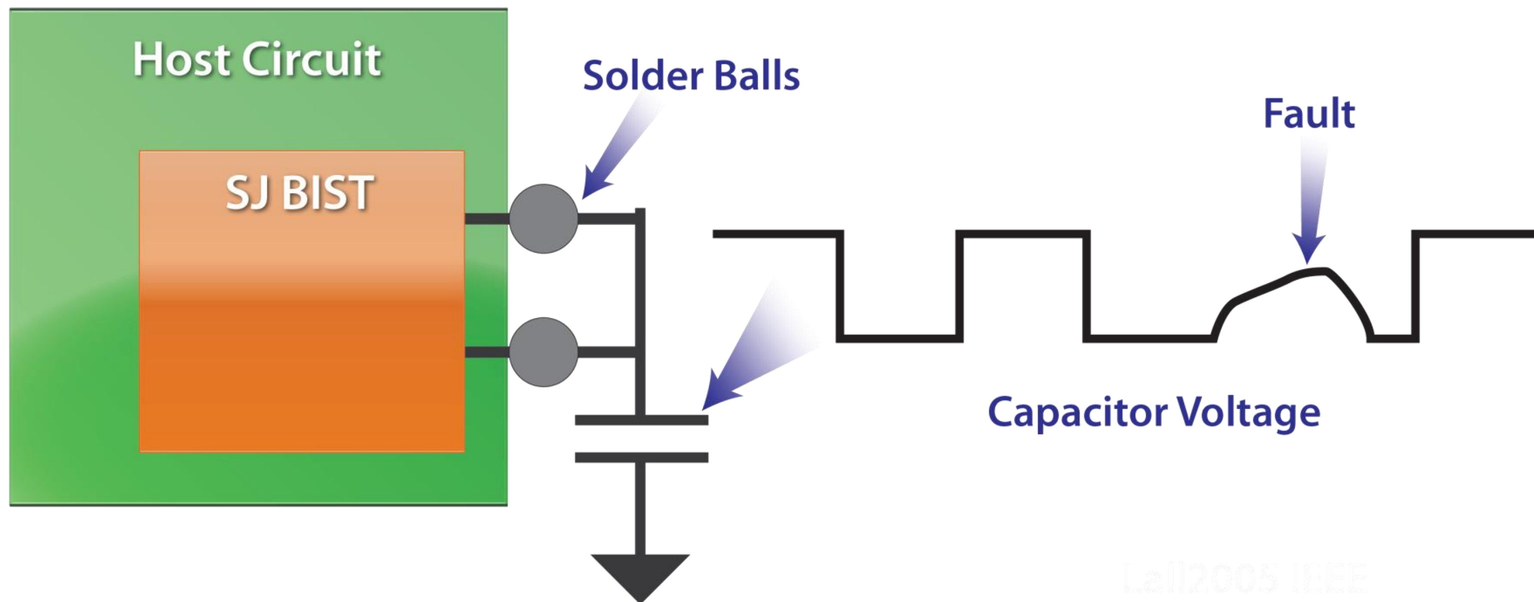
- SJ BIST = Solder Joint Built-in Self-Test
  - Original solution, enabling:
    - interconnect verification
    - validation of interconnect reliability
    - (life-time) monitoring of interconnect reliability
    - detection of intermittences
    - interconnect process qualification
  - Can be applied to validate the integrity and reliability of ***any type*** of interconnect

NTF Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST™ Operation

- Run Algorithm similar to a memory test: W0 – R0; W1 – R1
- Runs concurrently with host circuit
- Verilog/VHDL core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Uses interconnect resistance and capacitance



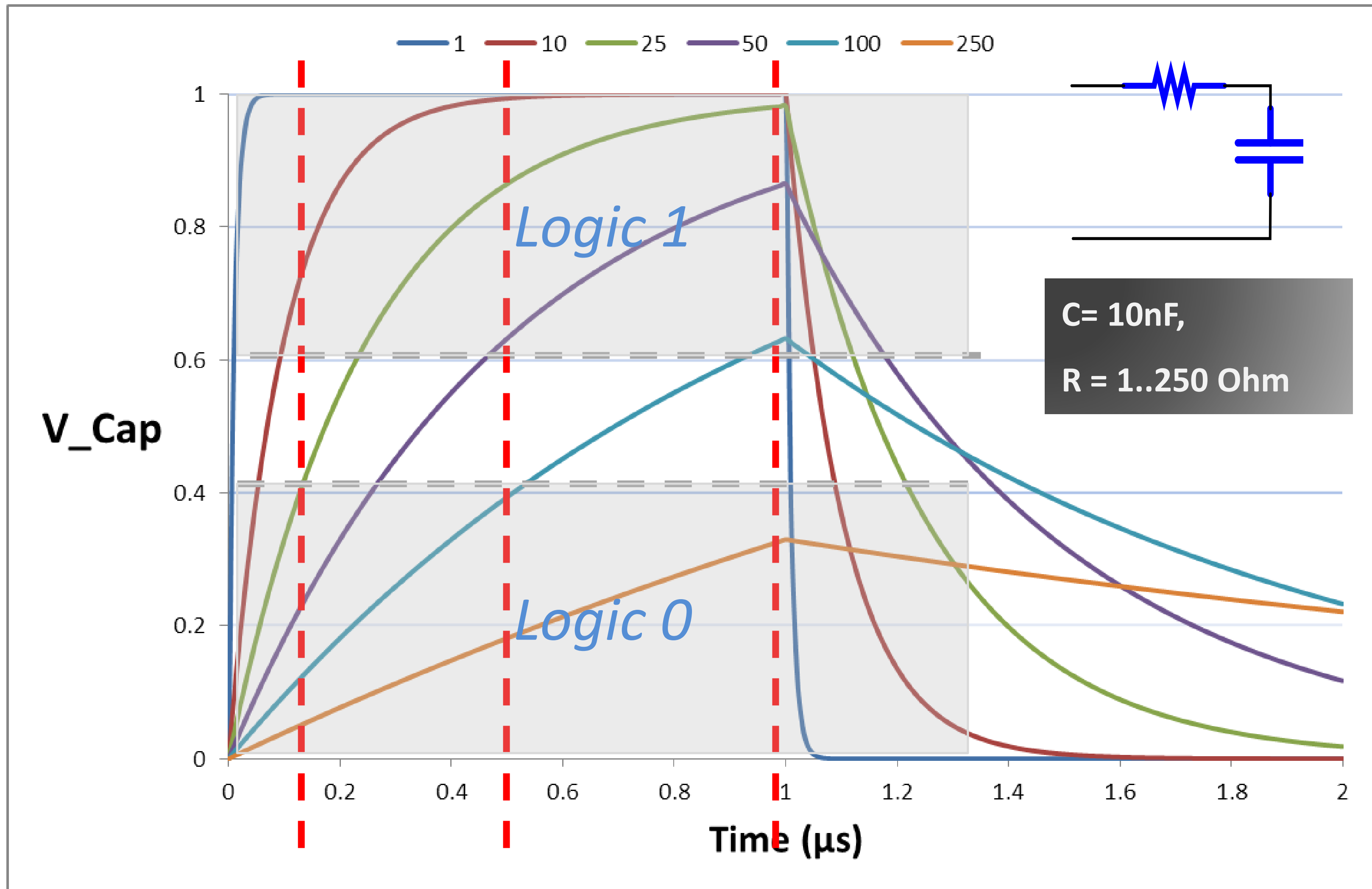
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Concept

- Interconnect == Memory
  - Connection between two dedicated pins
- Storage element == Capacitance of interconnect
  - Intrinsic (parasitic) capacitance of wire
  - I/O input capacitance
  - Small add-on capacitance
- Test == Transfer Charge == Memory Test
  - Write 0’s and 1’s
  - Verify if 0’s and 1’s are correctly stored

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Concept



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Concept

- Major players:
  - 2 dedicated host pins
  - Interconnect between pins
  - Interconnect capacitance
    - → intrinsic input capacitance + optional external cap
  - Interconnect resistance
    - → low resistance == OK
    - → increased resistance == Fault
  - Observation time
  - Continouous vs. scheduled test / observation

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Objectives & Features

- Objectives
  - Detection of impending interconnect failures
  - Unique in-situ testing in operating circuits
  - Technology-independent
- Feature and Benefits
  - Detects solder fractures prior to catastrophic failure of circuit
  - Detects changes in interconnect resistance
  - Provides actionable maintenance data
  - Independently tested and verified
  - Endorsed by leading automotive and aerospace customers

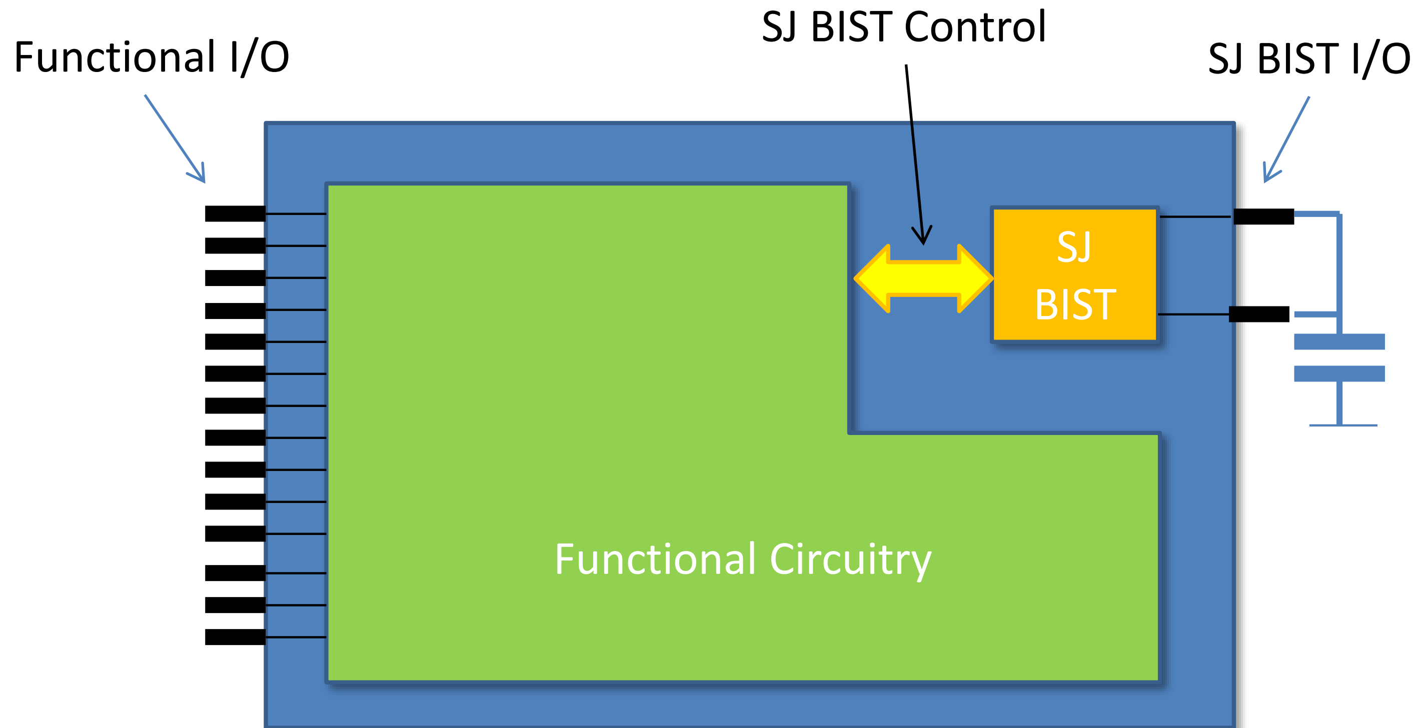
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Operation

- Independent
  - Concurrent & Continuously
    - → SJ BIST runs R/W tests as long as host circuit is powered on
    - → SJ BIST flags specified events
    - → Host inquires SJ BIST upon event or at specified time points
- Dependent
  - Host or Control unit enables SJ BIST at specific time points
  - SJ BIST runs for a specified amount of time
    - → SJ BIST flags specified events
    - → Host inquires SJ BIST

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

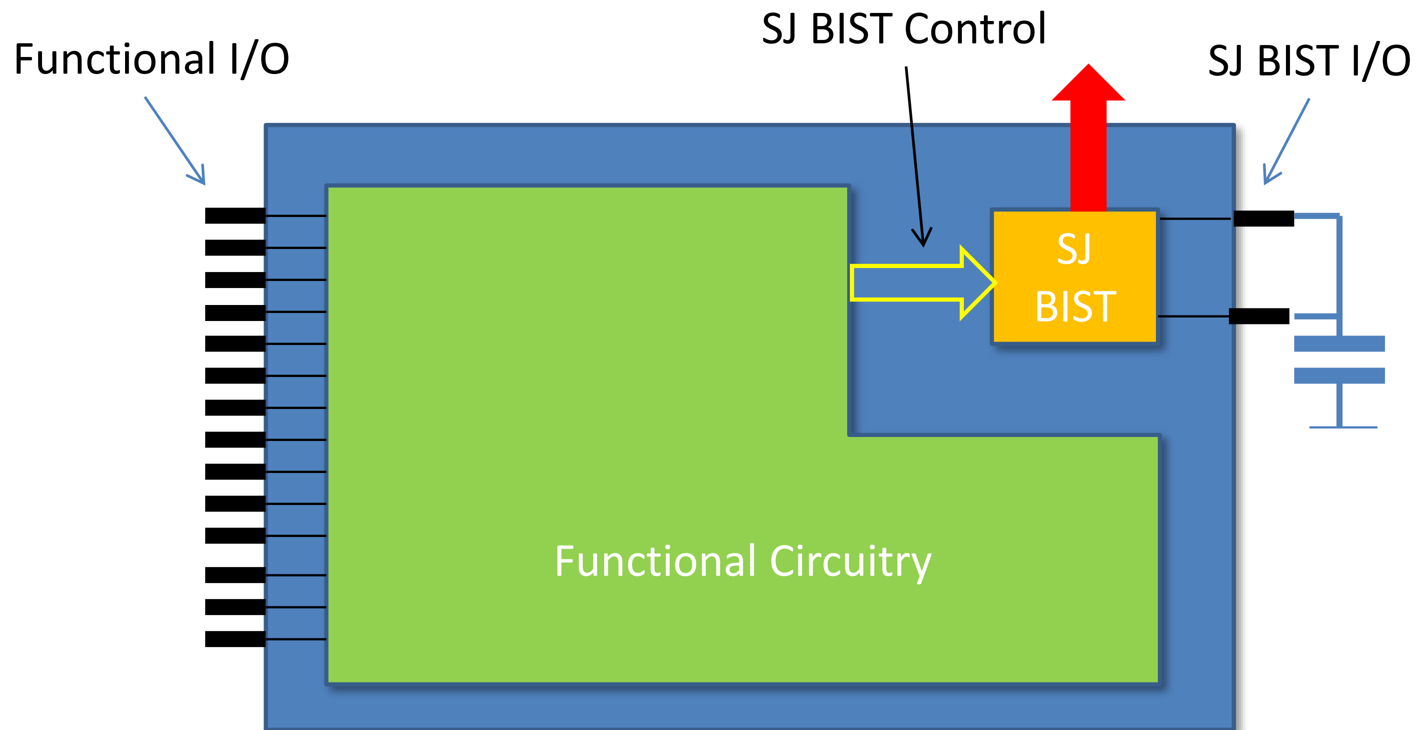
SJ BIST Implementation



- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/0

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

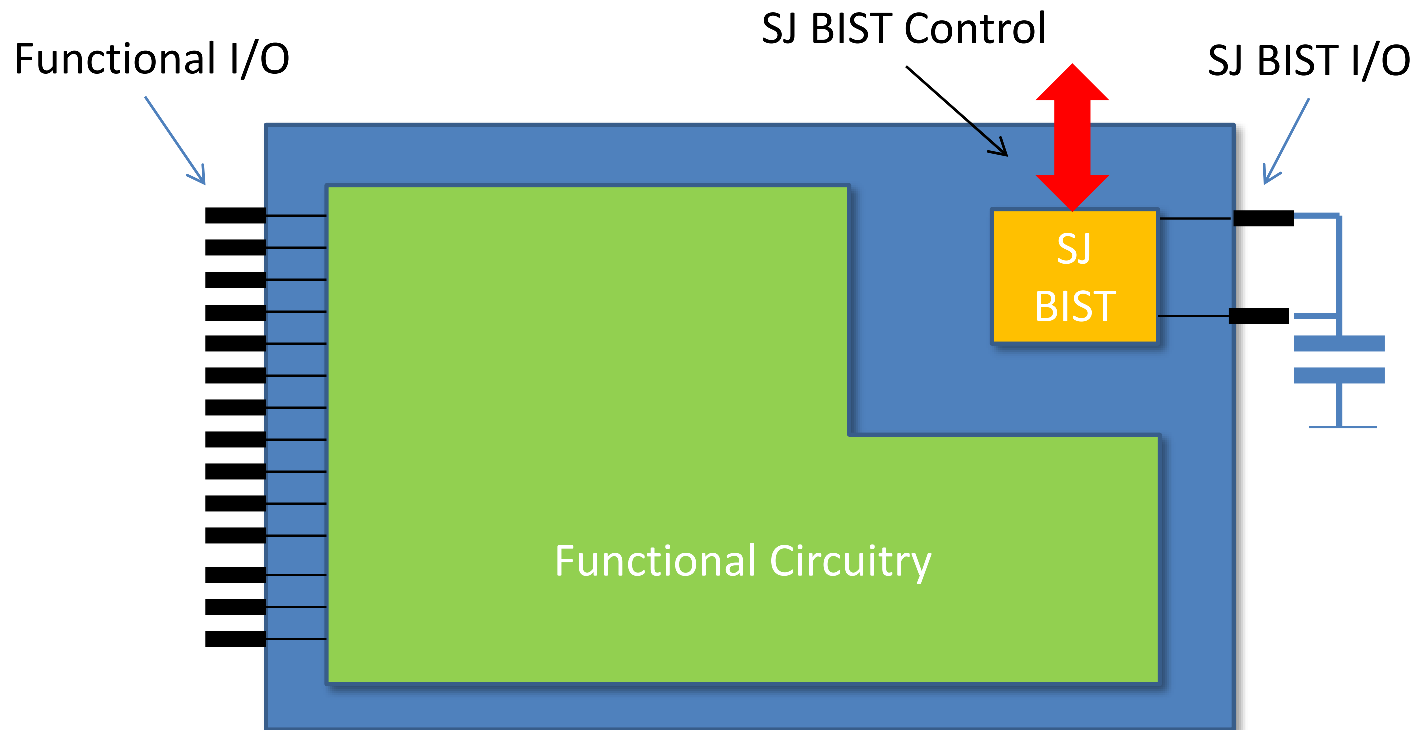
SJ BIST Implementation



- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/O

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Implementation



- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/0

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Information

- Flags:
  - Permanent vs Intermittent fault
  - Flags can be treated individually or combined in a global Pass/Fail flag
  - Provide "occurence" information
- Event Counts
  - # of occurances of a permanent or intermittent fault during a given timeframe
  - Provide "severity" information
- Flags & Event counts are associated to each SJ BIST Test pin

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST & Detection of Failures

- Detection of Intermittent faults
  - SJ BIST can detect events that are lasting less than 10ns
  - SJ BIST can detect resistance increases of 10Ω or less
  - Detection is function of SJ BIST operating frequency, interconnect capacitance and interconnect resistance
- Fault detection is linked to SJ BIST configuration.

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST & Detection of Failures

- Detection of Degradation
  - Interconnect degradation will result in permanent or intermittent fault introduction.
  - Test results will evolve from “good” to “fail”
  - If SJ BIST runs continuously a flag will be raised upon the occurance of a fault
  - Failure time point (moment when the flag is raised) is function of SJ BIST configuration and hence tunable by the user.

NTF
Nordic Test Forum

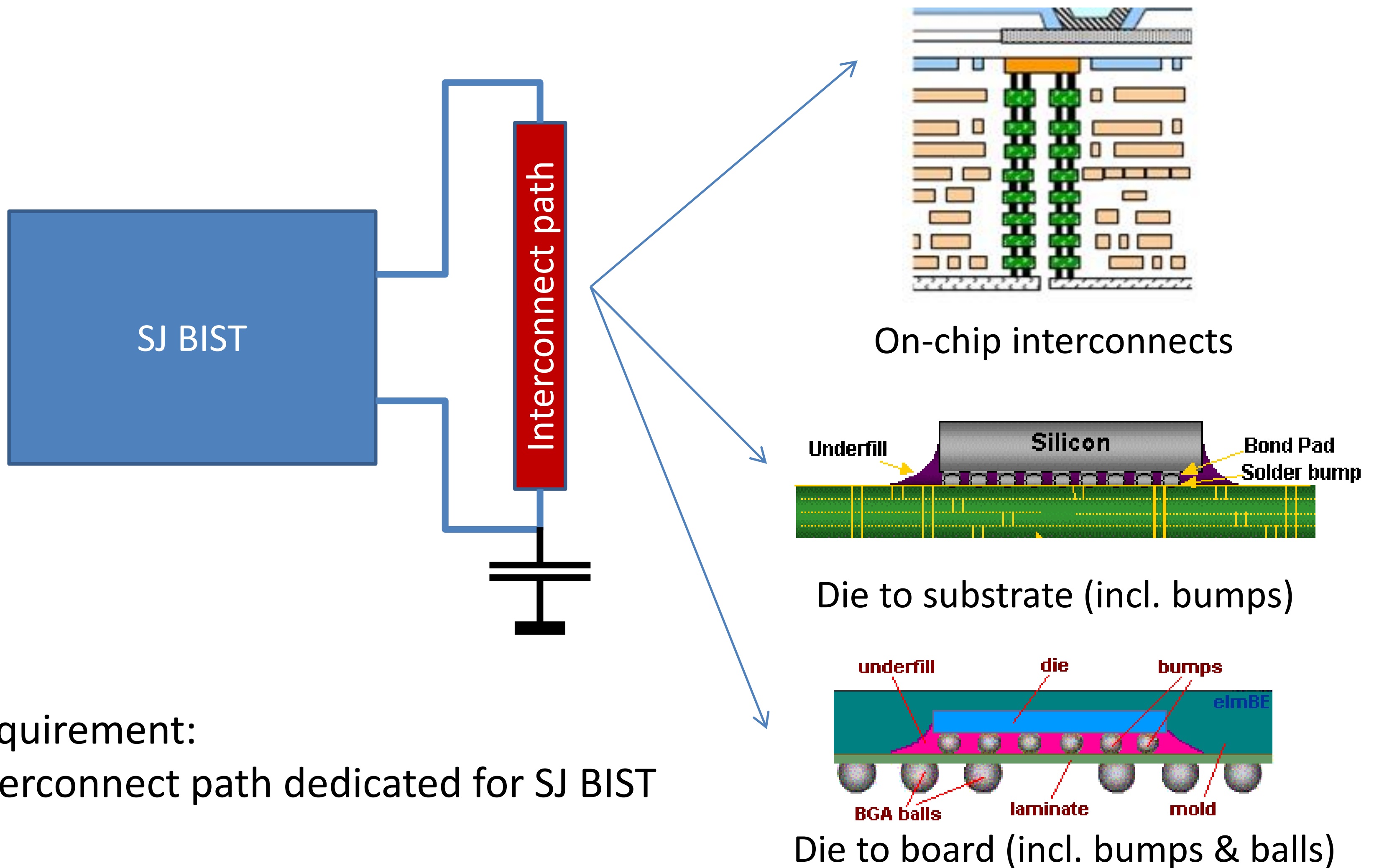
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Applications

- Interconnect validation & monitoring
  - From on-chip interconnects to cable testing
- Assembly (solder) process qualification
  - From die stacking to system assembly
  - LT/ALT/HALT testing
- Package qualifications
- Die handling – Crack detection
- Assembly monitoring
  - In field testing
- Validation of packaging solutions & techniques
- … and many more

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Application



On-chip interconnects

Die to substrate (incl. bumps)

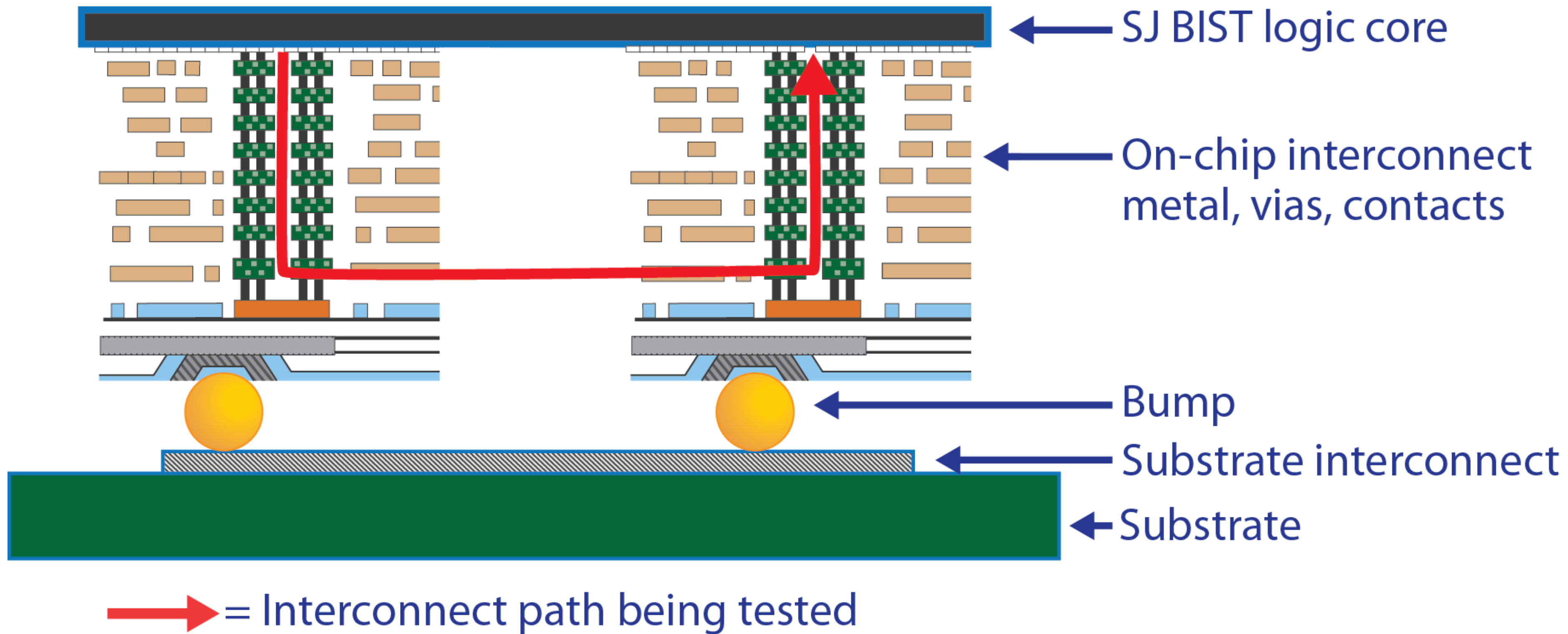
Die to board (incl. bumps & balls)

Requirement:
Interconnect path dedicated for SJ BIST

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Application

Testing On-chip Interconnect

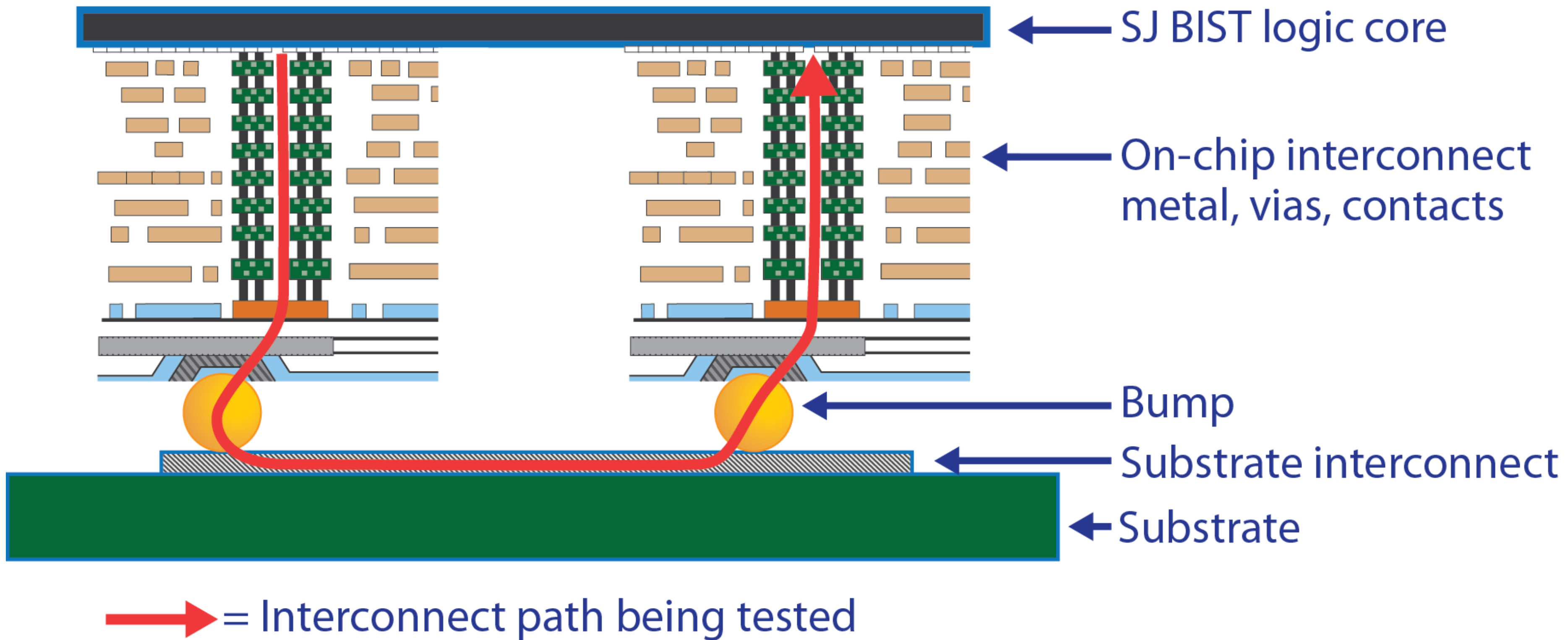


Need for dedicated on-chip path between SJ BIST™ Observation pins

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Application

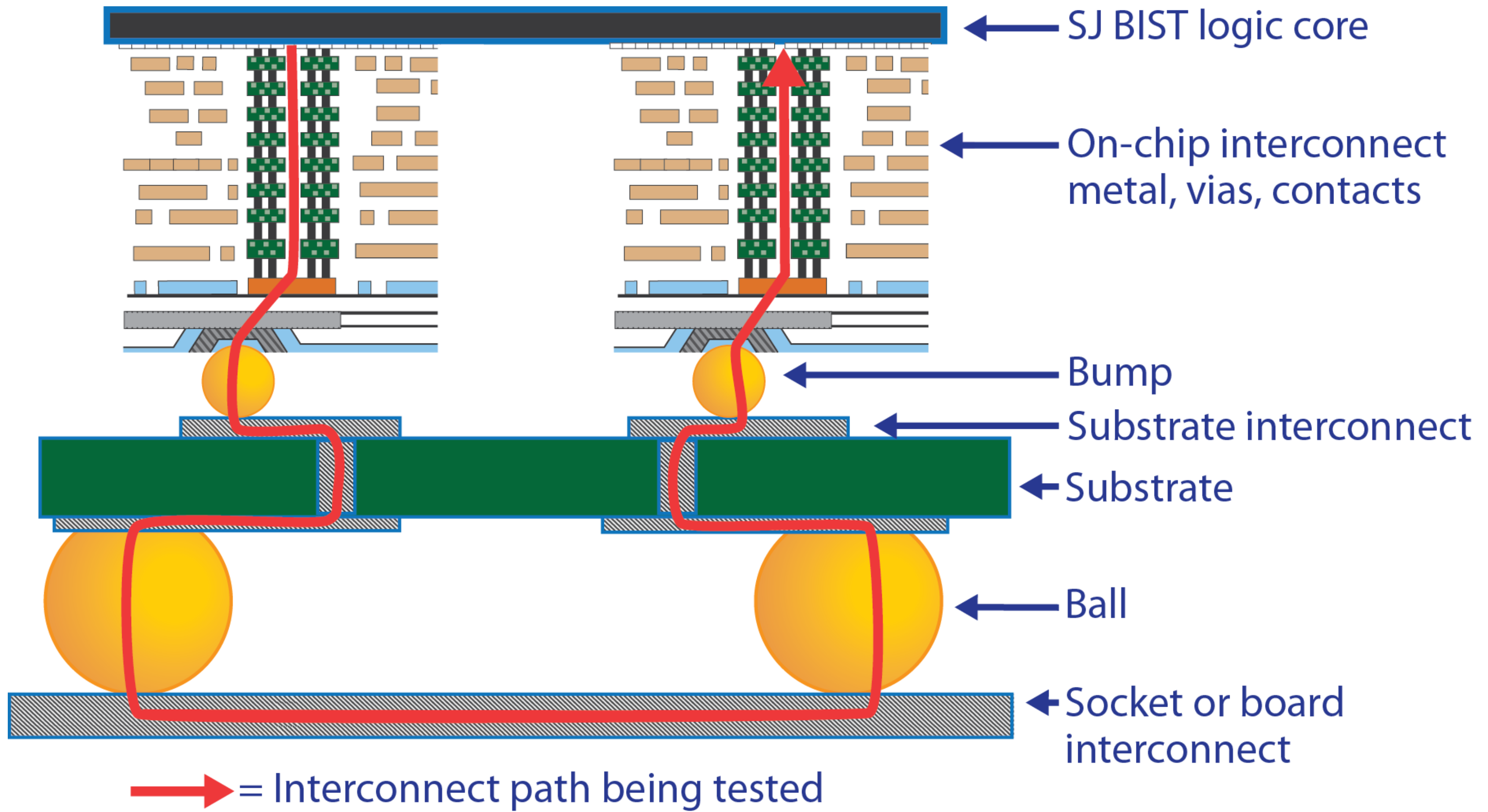
Testing Die to Substrate



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Application

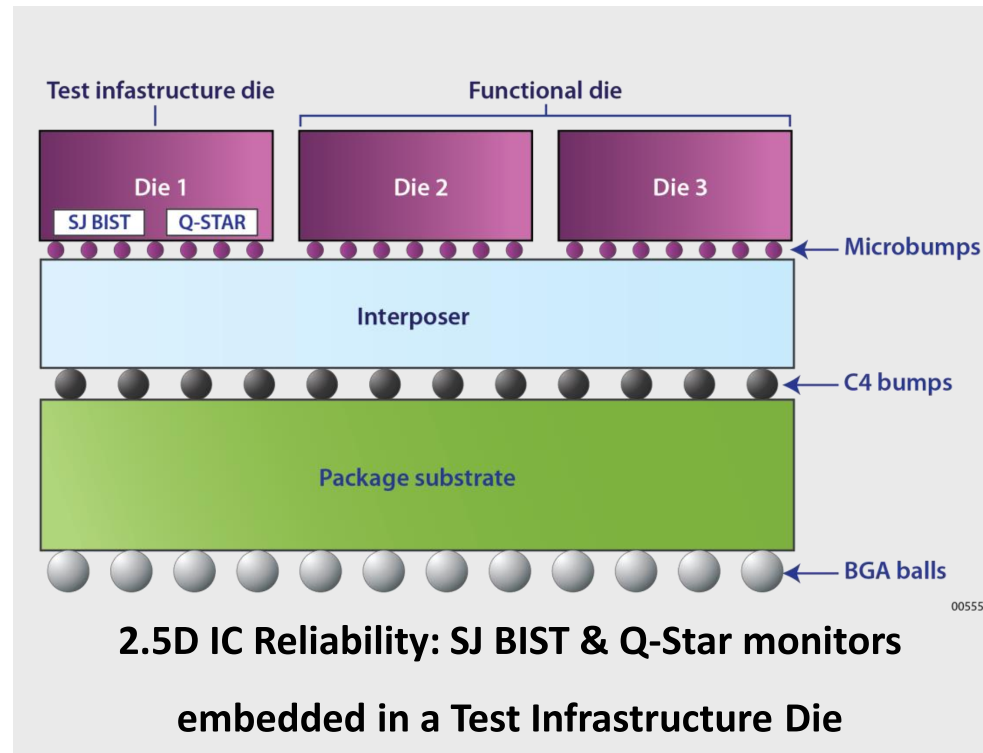
Testing Die to Board



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

2.5D IC Reliability: Test Infrastructure Die

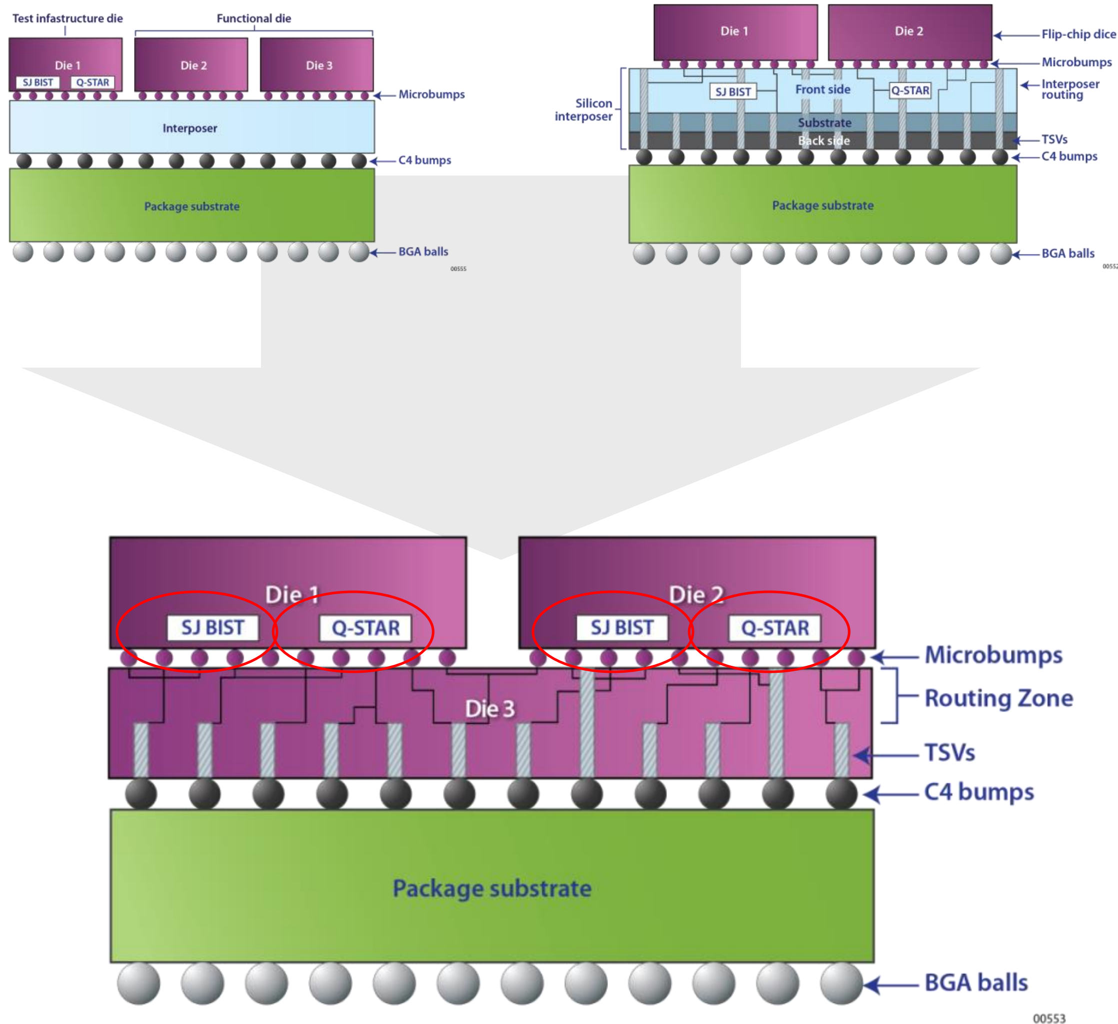
- "Test Infrastructure" die: Connects to strategic traces routed through the interposer
  - Most critical functionality
  - Most sensitive to degradation (e.g., corners or centers of Die 2 or Die 3)
  - Can monitor many signals
- SJ BIST/Q-Star IP embedded in Test Infrastructure die
- Advantages
  - Minimizes interposer overhead
  - Low cost IC
  - Upgrades are simple
- Disadvantages
  - Extra interposer real estate
  - Distance from some signals



2.5D IC Reliability: SJ BIST & Q-Star monitors embedded in a Test Infrastructure Die

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

From 2.5D IC to 3D IC Reliability Monitoring

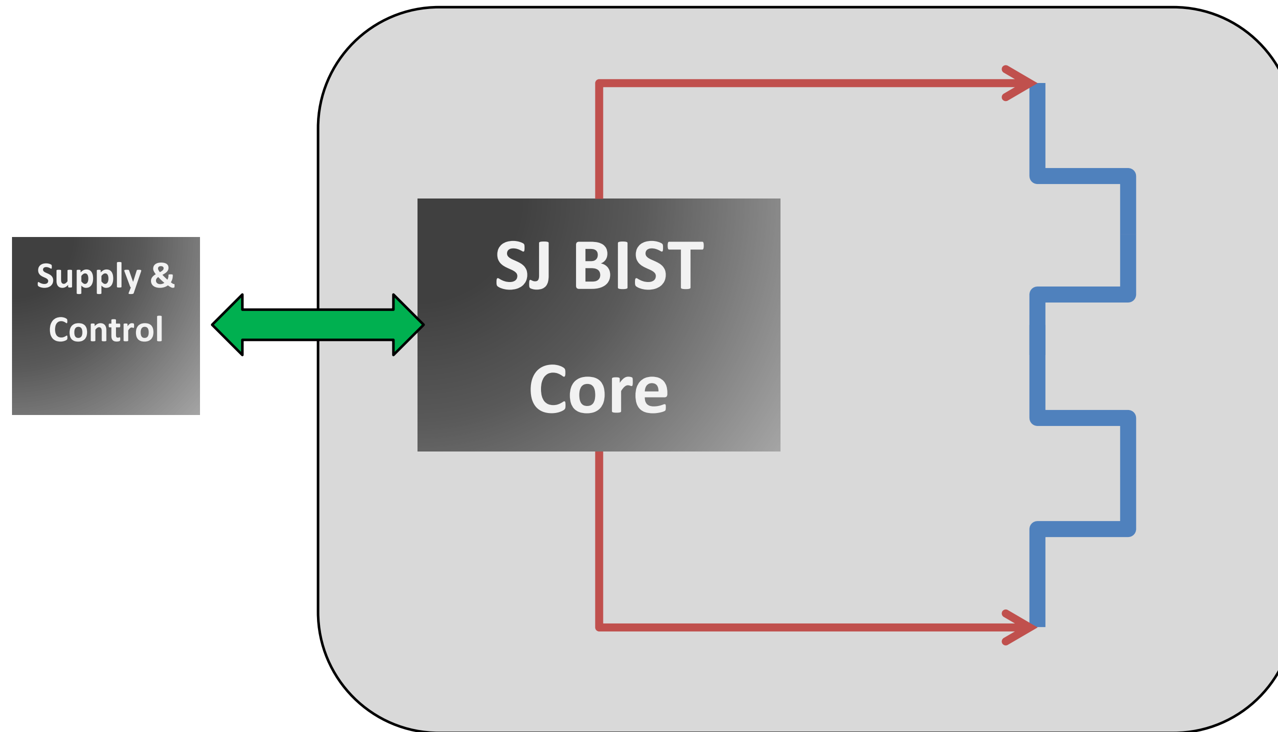


- 3D IC migration: Embed SJ BIST / PGMon IP in TSV-enabled ICs
- Required when no interposer present Highest quality monitoring
- Reduces cost and overhead
- Standardized approach for broadest applicability

NTF Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

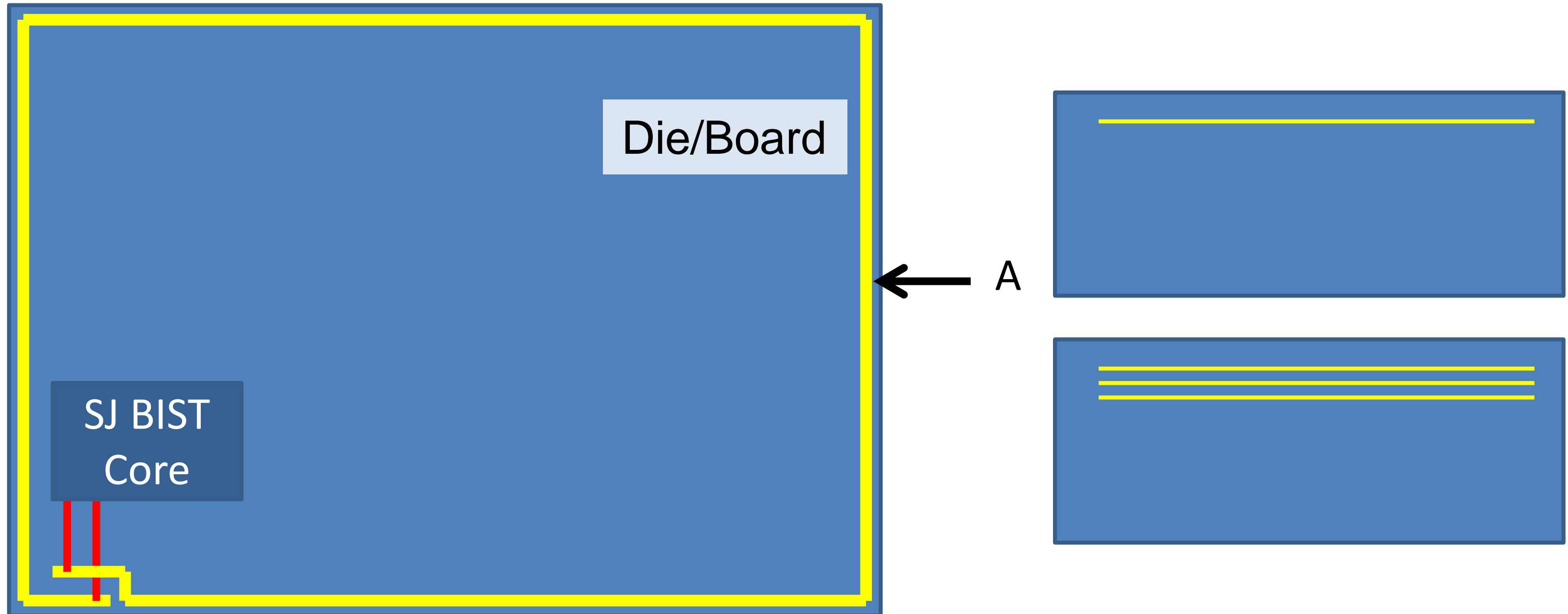
Die Crack Detection - Option A



- Test structure & monitor are part of the same die

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

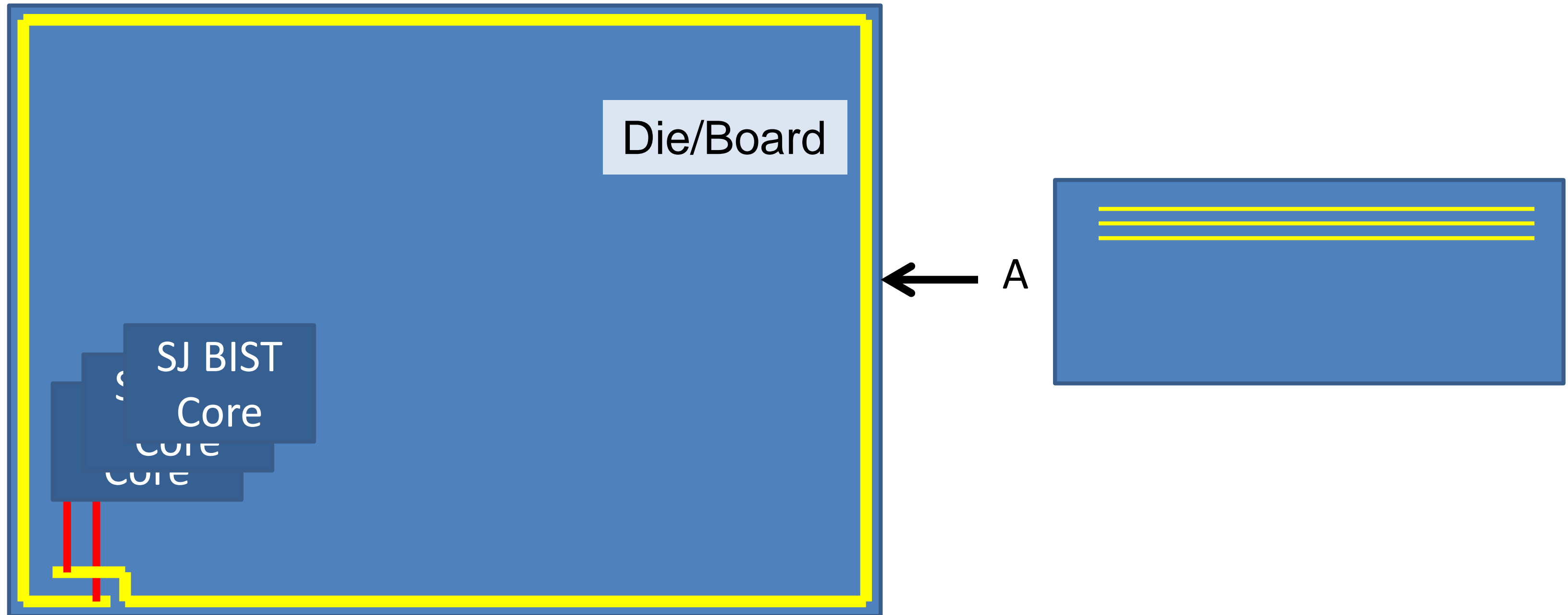
Die/Board Crack Detection - Simple Ring Structure



Structure runs on the edge of the die or board and could either be a single layer or a multilayer structure observed by a single SJ BIST core

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Die/Board Crack Detection - Simple Ring Structure – 2

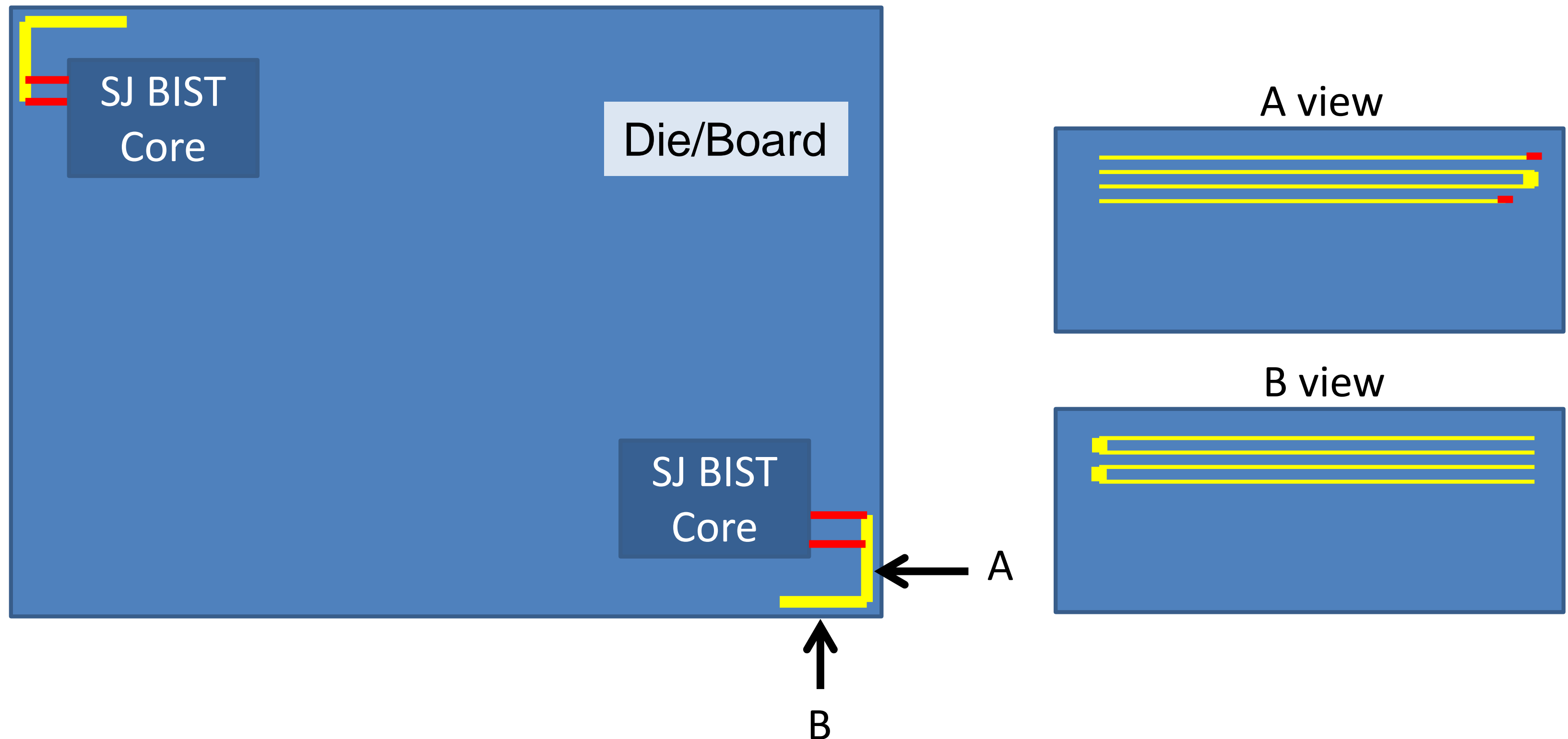


Multi-Layer Structure runs on the edge of the die or board

Each layer is observed by a specific SJ BIST core

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Die/board Crack Detection - Corner Structure

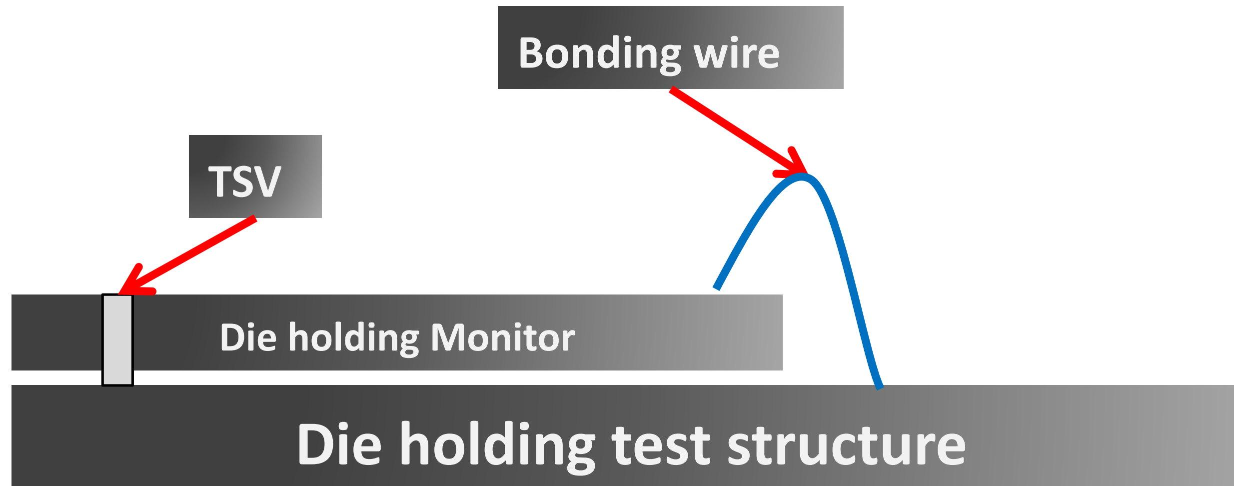


Multi-Layer Structure linked to the corners of the die or board

Each structure is multilayer and is observed by a specific SJ BIST core

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

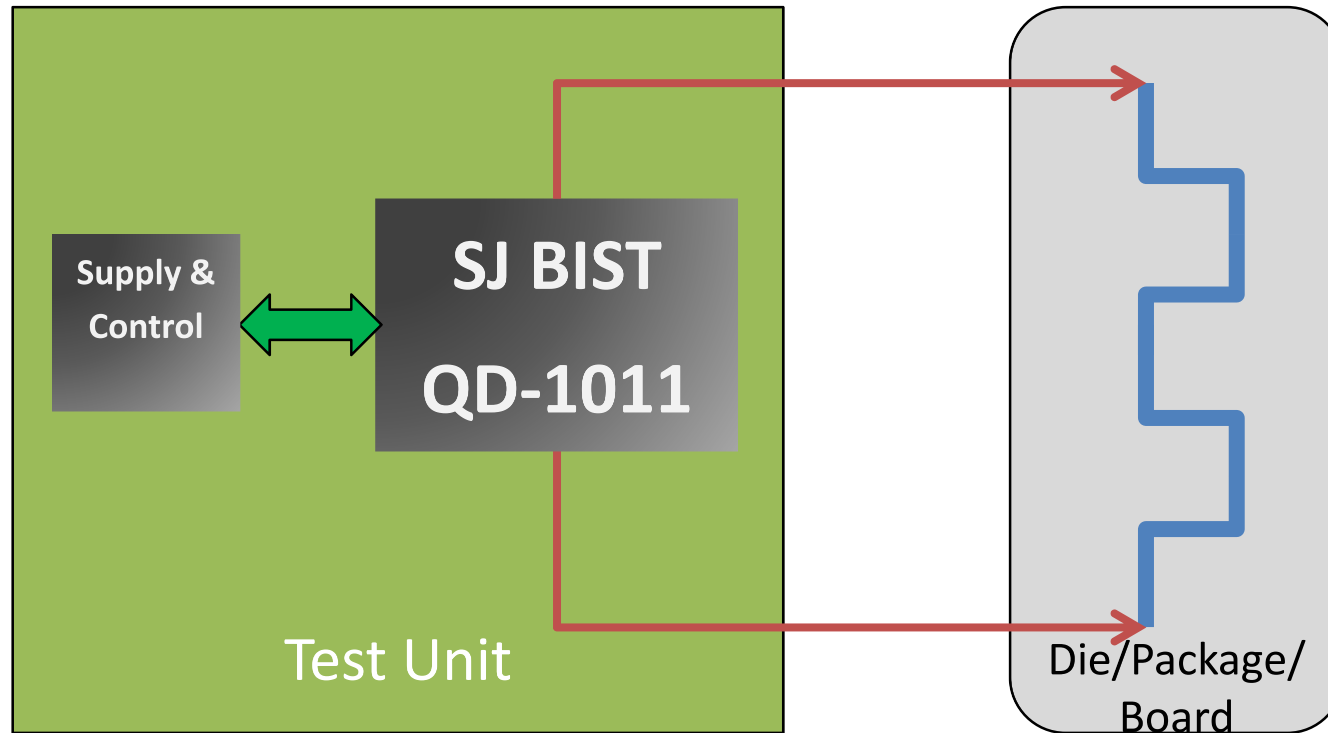
Die Crack Detection - Option B



- Test Structure & monitor are on separate dies

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

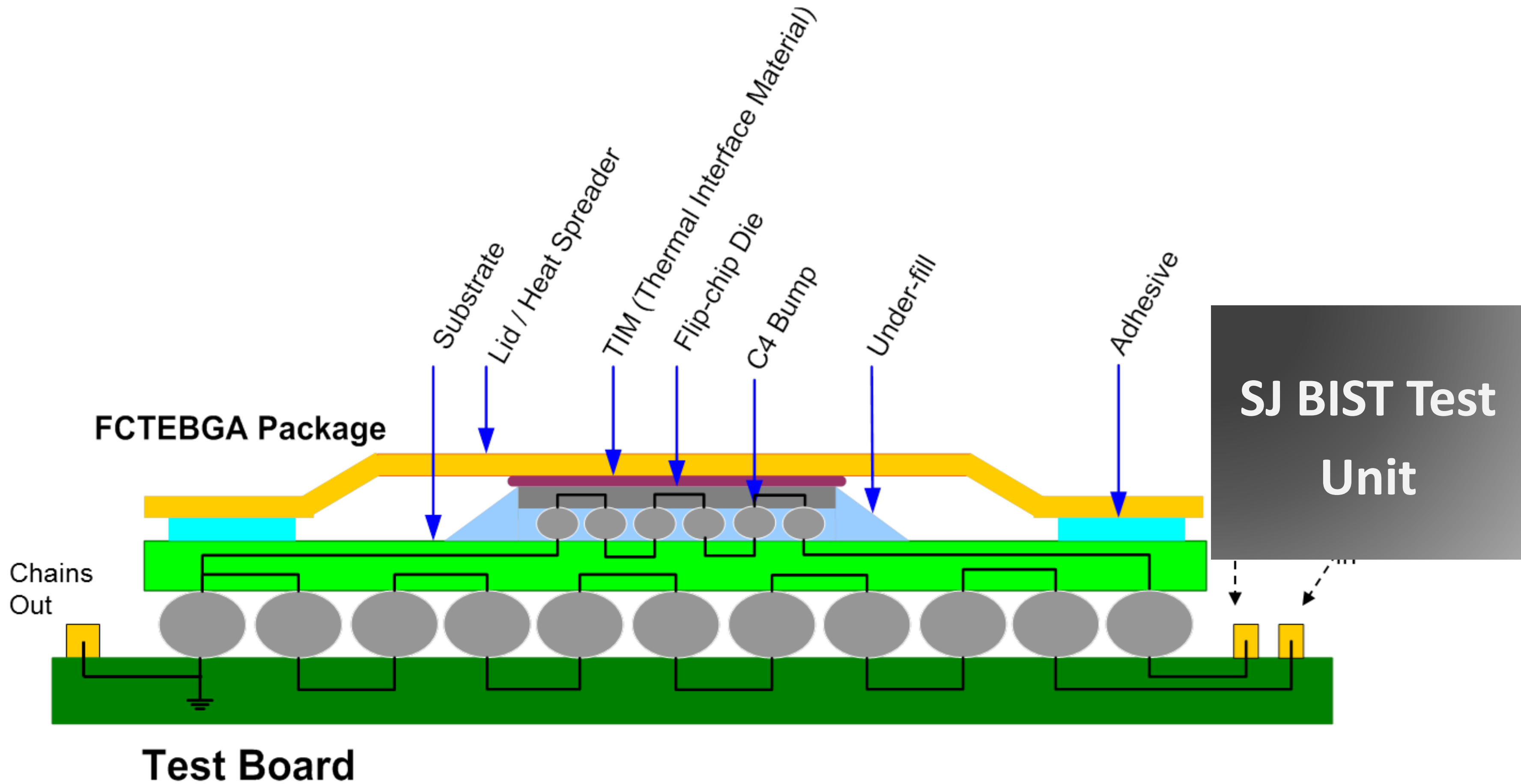
Crack Detection - Option C



- Test structure and external test equipment

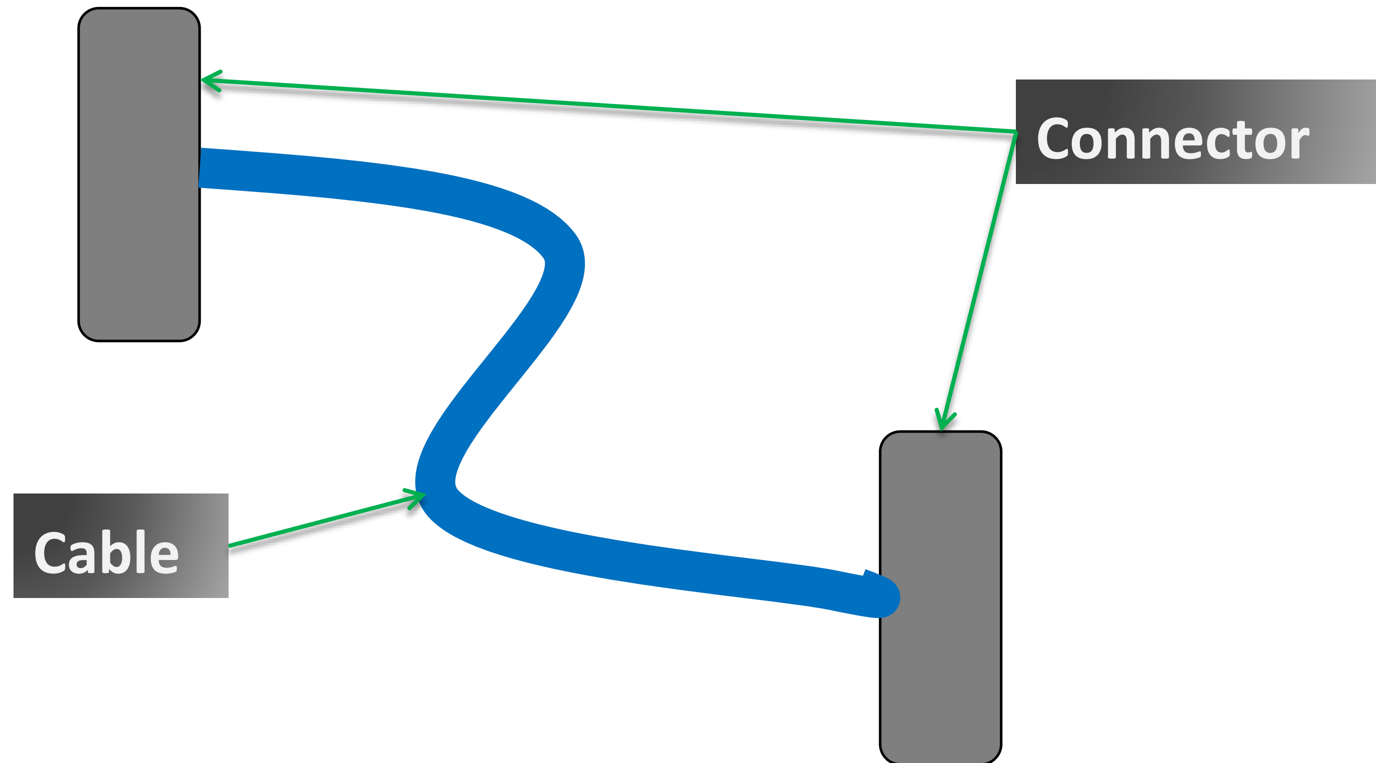
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Daisy Chain Revisited



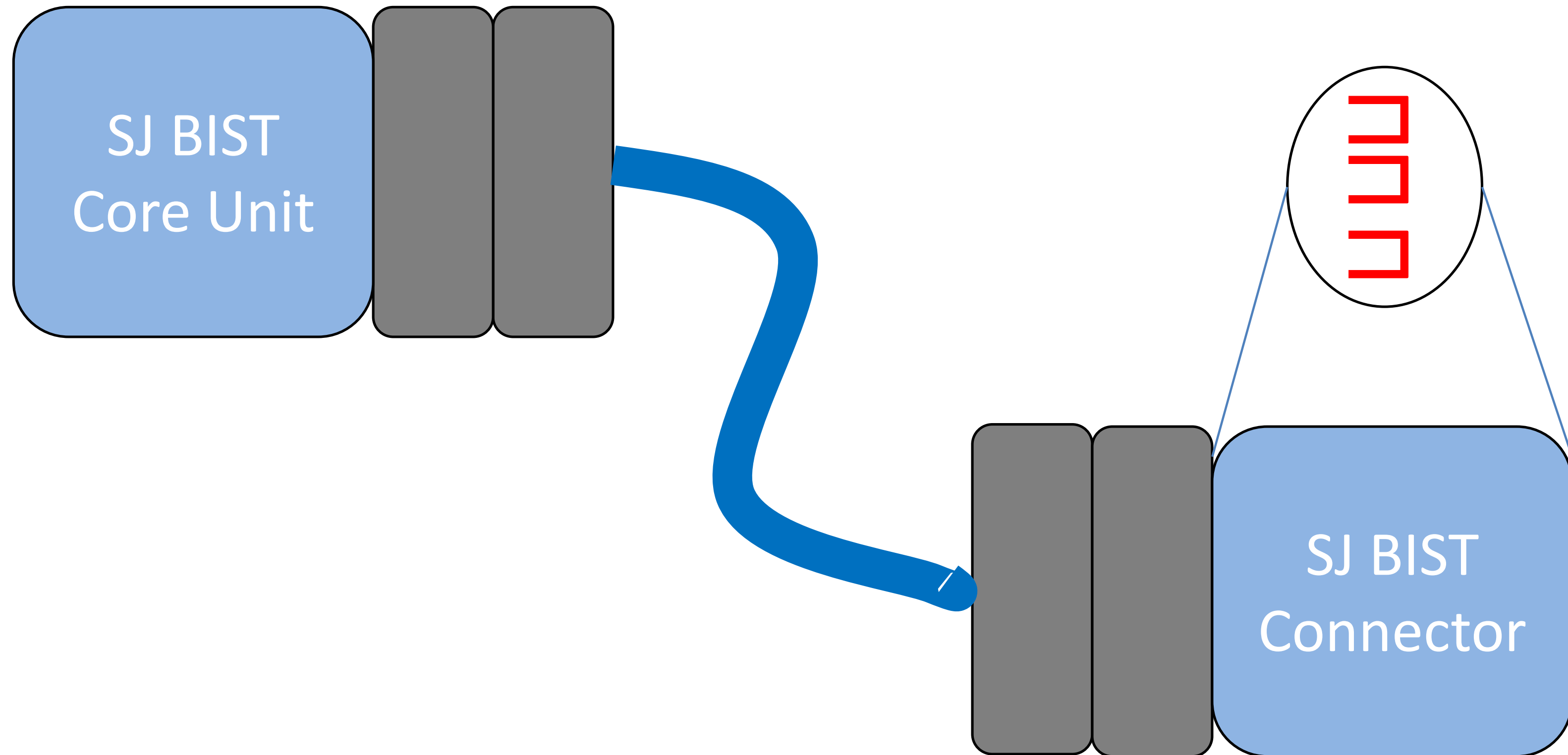
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Testing Cables



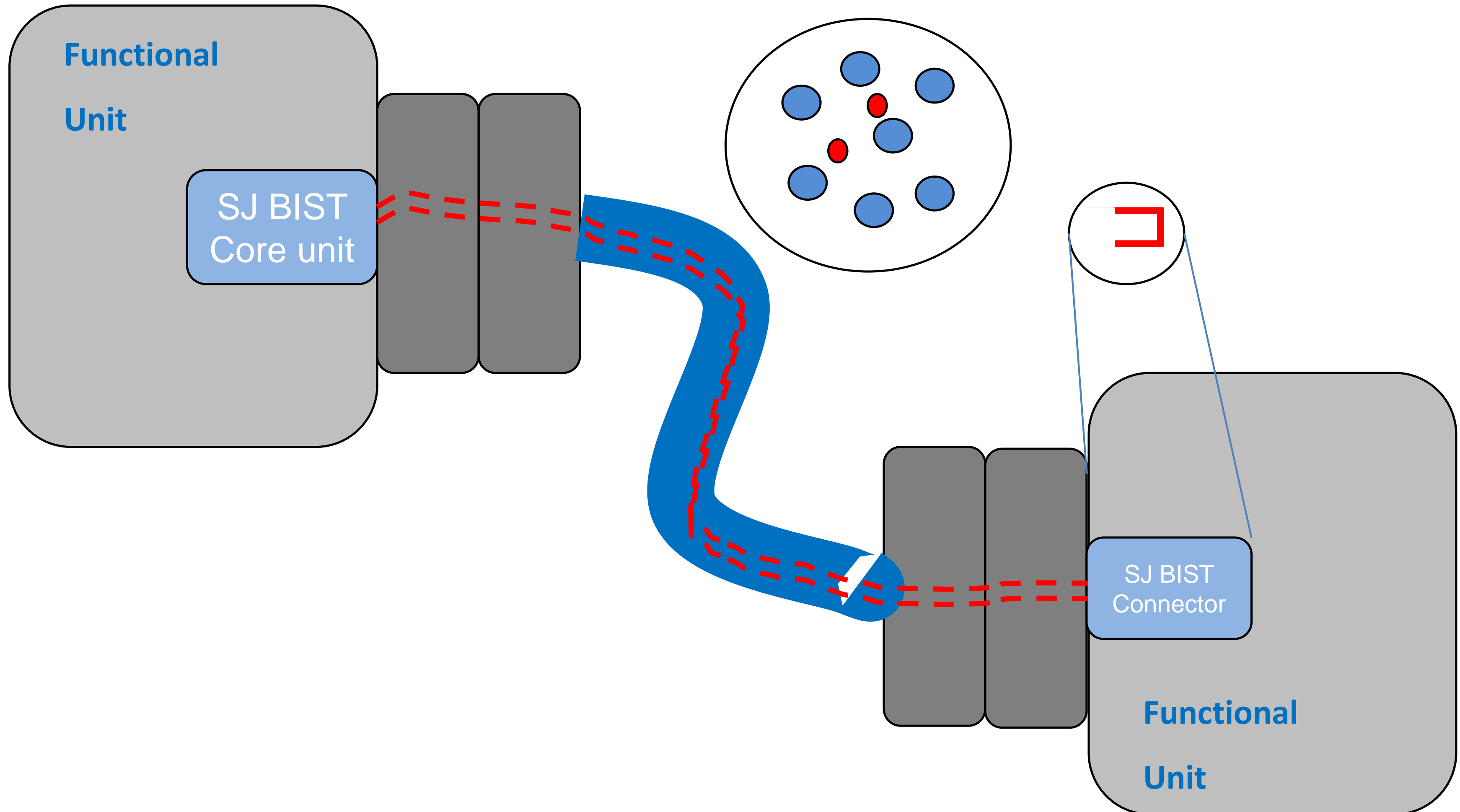
© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Testing Cables



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Monitoring Cables



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

SJ BIST Demonstration/Evaluation Kit

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect ePHM - Application Case

- **Customer**
  - BAE Systems, Johnson City, NY.
- **Problem**
  - Issue of missions failure due to early FPGA failure.
  - Solder joints of BGA packages experience thermo-mechanical stresses causing accumulative fatigue damage.
  - Fatigue damage results in spikes of high resistance of increasing frequency and duration as the damage increases.
  - The high resistances cause intermittent incorrect levels of signals – as a result, a logical 0 or 1 can be incorrectly set or reset.
- **Solution**
  - Sentinel Interconnect HALT based on deploying SJ BIST during HALT testing of problem board, serving early detection of manufacturing issues and to qualify electronic boards for military-aerospace use

NTF Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Interconnect ePHM - Application Case

- **Customer**
  - ST Microelectronics – Dallas, TX
- **Problem**
  - Package qualification
  - Limited timing resolution of event detection units
- **Solution**
  - Configurable SJ BIST Solution
  - Considerably improved detection capabilities of short term intermittences (events) as well as increased resolution of determining degradation resistance.

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Summary

- SJ BIST
  - Flexible and versatile tool for Interconnect monitoring at time zero and during product lifetime
  - Small core (about 100 eq gates)

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Thank you!

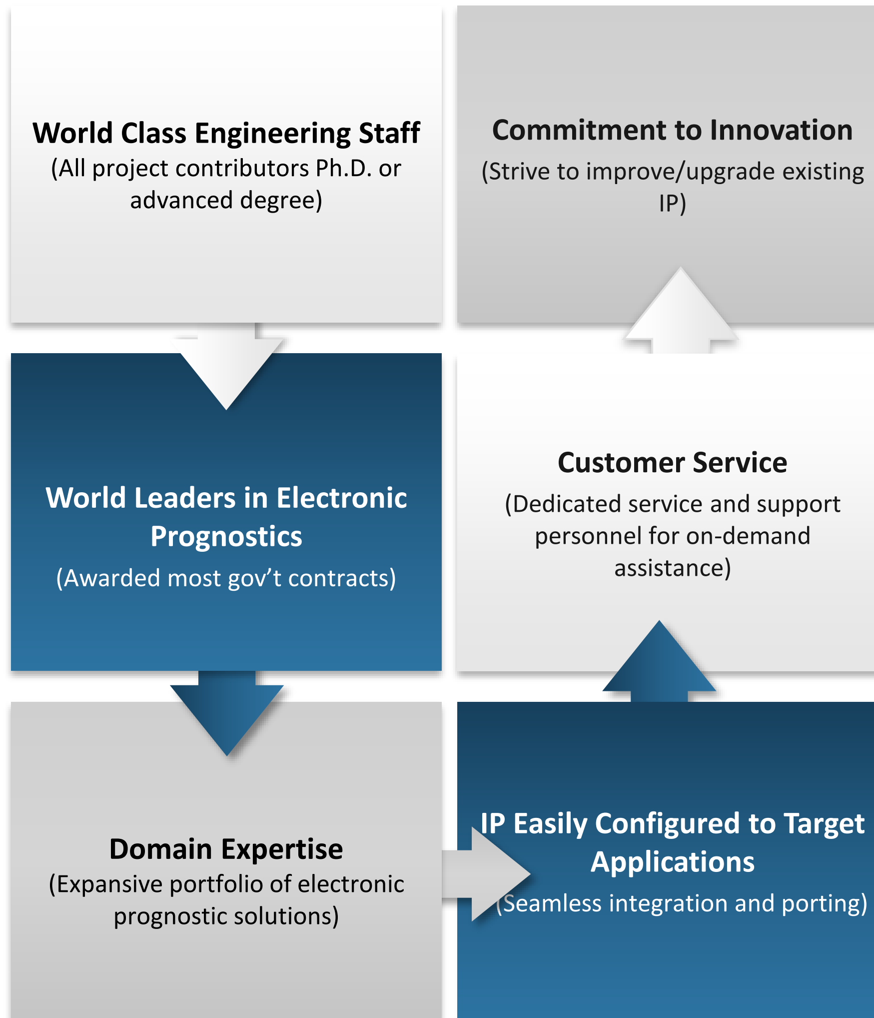
Ridgetop Europe nv

Hans Manhaeve
CEO/CTO
hans.manhaeve@ridgetop.eu
+32 50 315744 (office)
+32 478 331003 (mobile)

NTF
Nordic Test Forum

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

Ridgetop Delivers



© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential

About Ridgetop

- Ridgetop Europe (formerly Q-Star Test) with HQ in Brugge, Belgium
- Ridgetop Group with HQ in Tucson, AZ.
- Microelectronic Design and Test Solutions:
  - SJ BIST™ Based Test Solutions
  - ProChek™ Semiconductor Characterization System
  - Q-Star Test™ Precision Current Measurement Instruments
  - PDKChek™ In-Situ Test Structures
  - ISO:9001/AS9100C-compliant Design and Integration Services
- Strong market position with commercial and government customers in USA, Canada, Europe, and Asia

Ridgetop Group Facilities in Tucson, AZ

Ridgetop Europe Facilities in Brugge, Belgium

© 2016 – Ridgetop Europe & Ridgetop Group – all rights reserved – copying or distributing without written permission is strictly forbidden – Confidential