Board and SoC Test Instrumentation for *Ageing* and *No Failure Found*

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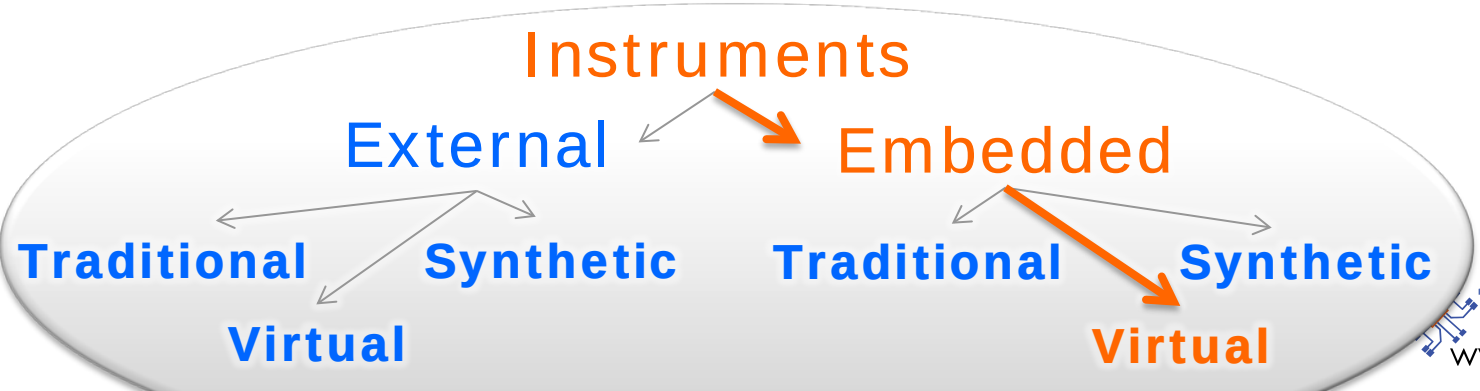
Testonica Lab

About Testonica Lab

- ChipVORX (in cooperation with GOEPEL electronic) is:
  - a library of ready-to-use ***embedded virtual*** instruments
  - a technology for *automatic control* of embedded instruments using the standard 1149.1 JTAG port
  - improves test coverage/quality/speed
- Testonica invented ***embedded virtual*** instrumentation
  - The only provider of this type of instrumentation (EU+US pat.)
  - Allows a fully automated "push-button" solution



Presentation Outline

- No Failure Found problem
- Embedded Instrumentation
- EU funded FP7 project BASTION
- Conclusions
- Extra: Ageing Failure Resilience with P1687

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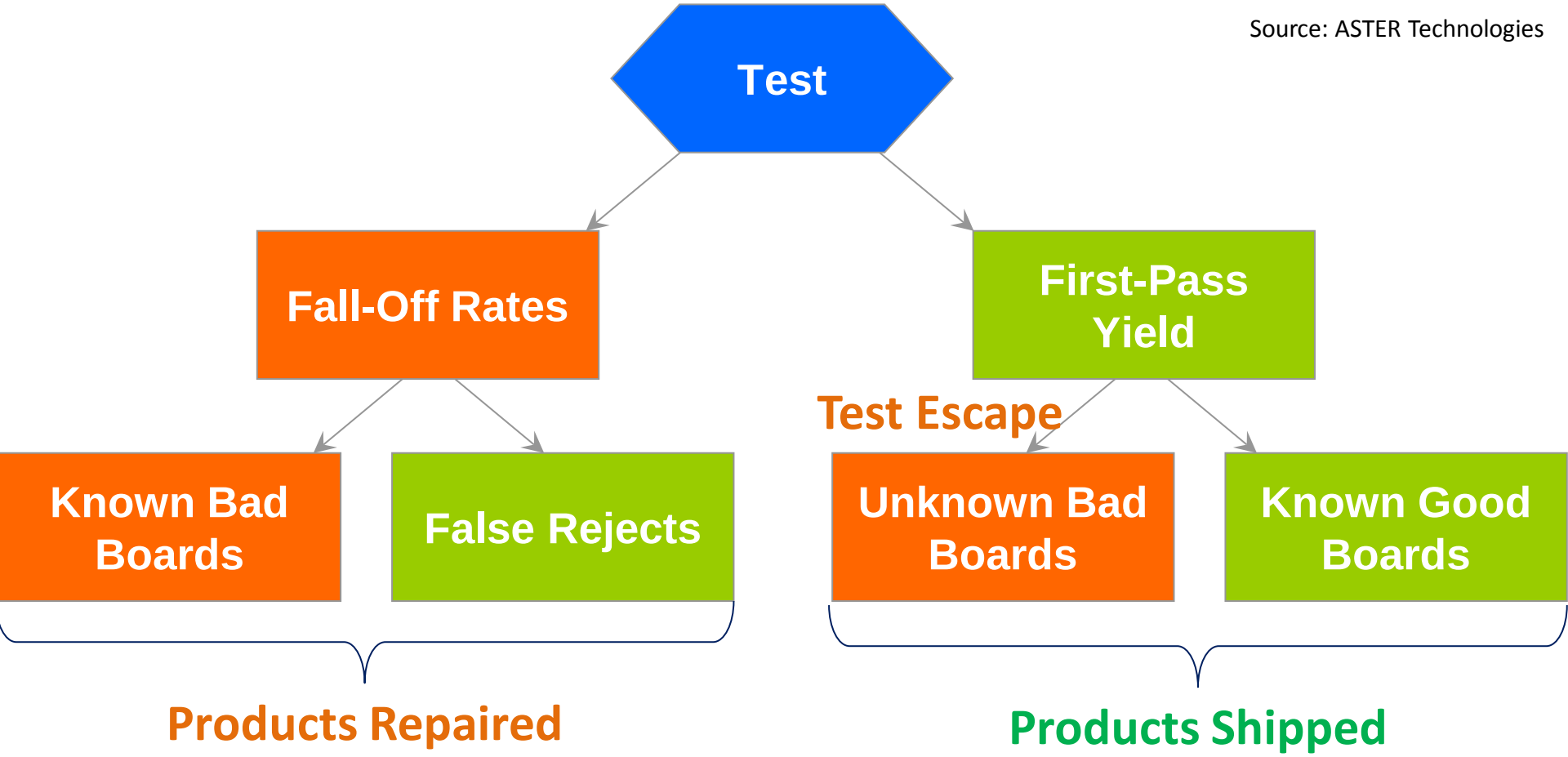
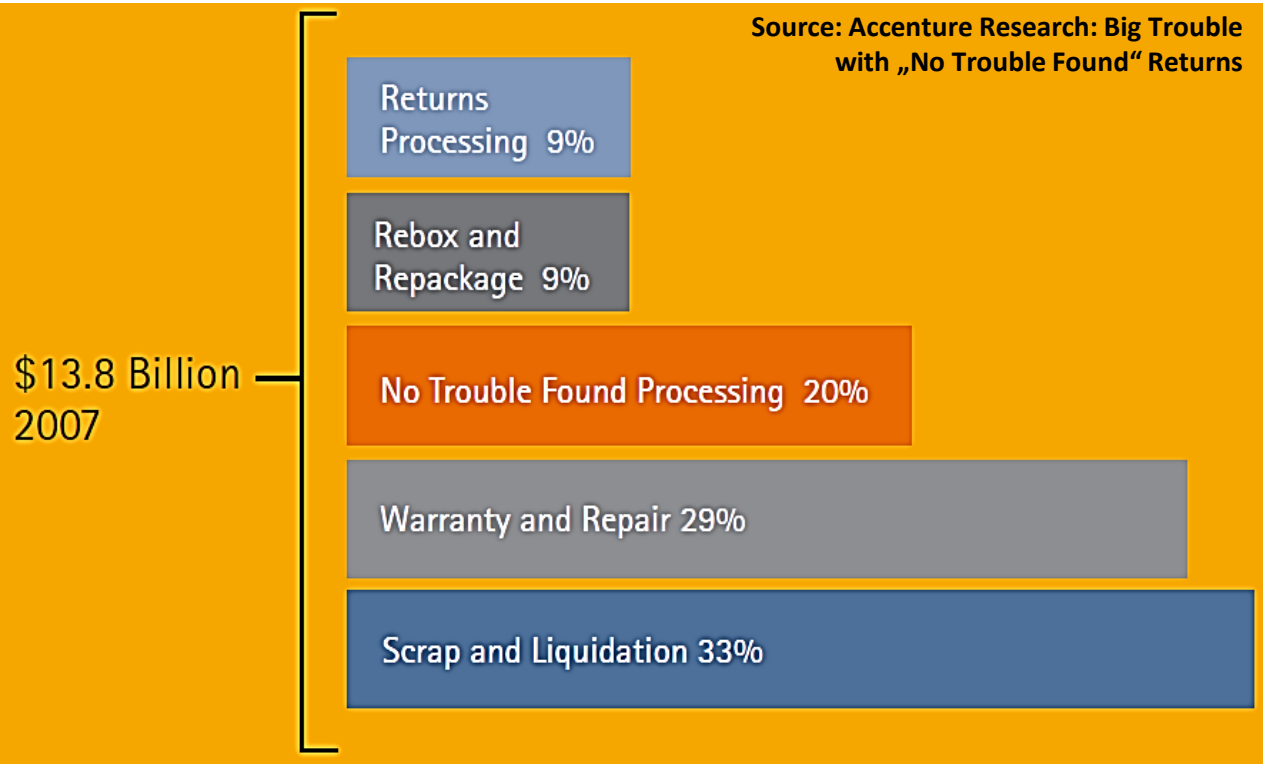
Test Escapes and No Failure Found

Source: ASTER Technologies



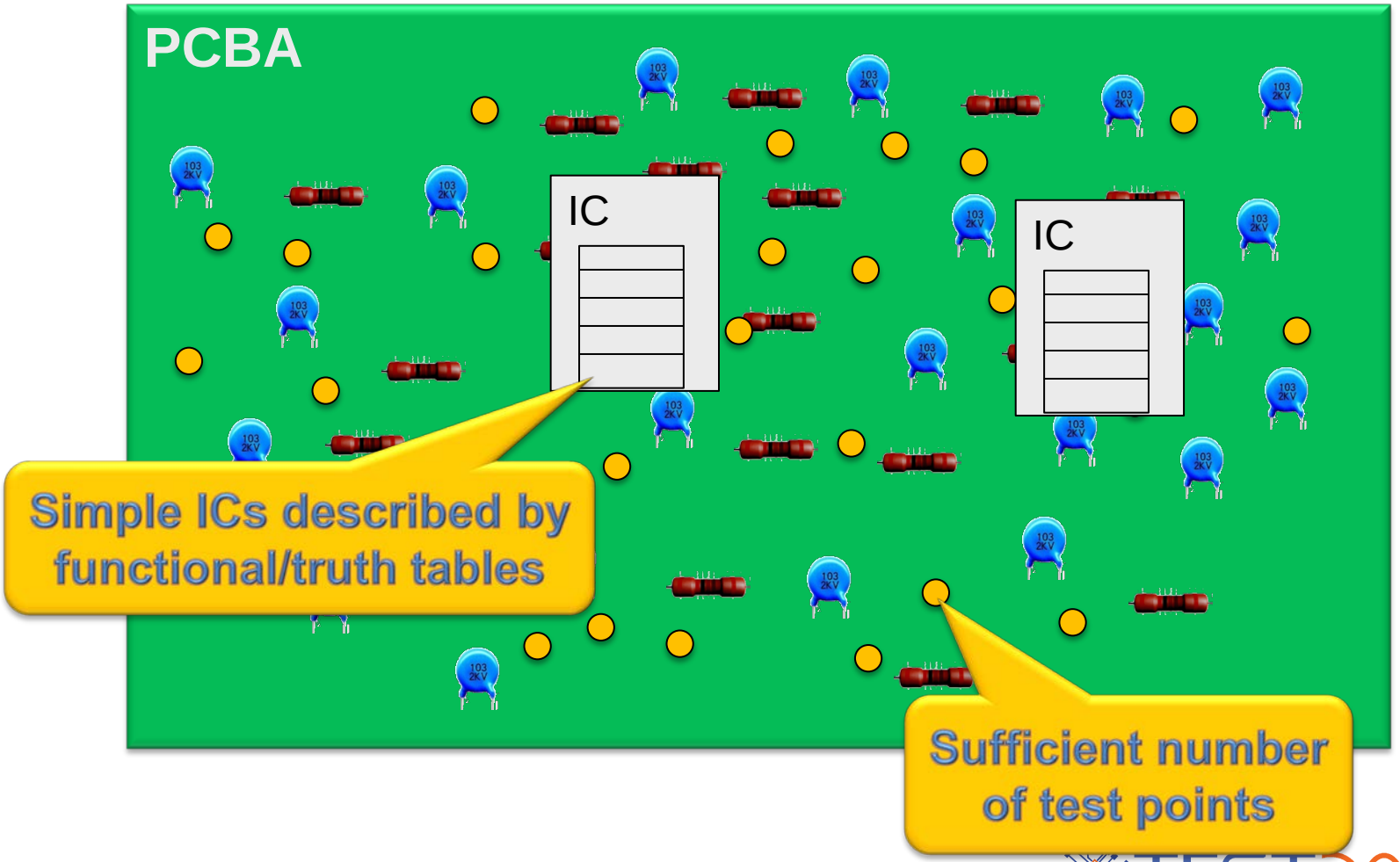
No Failure Found – NFF

- NFF symptoms (product level)
  - System passes all tests at the production
  - System fails at the customer
  - Troubleshooting cannot repeat the failing condition

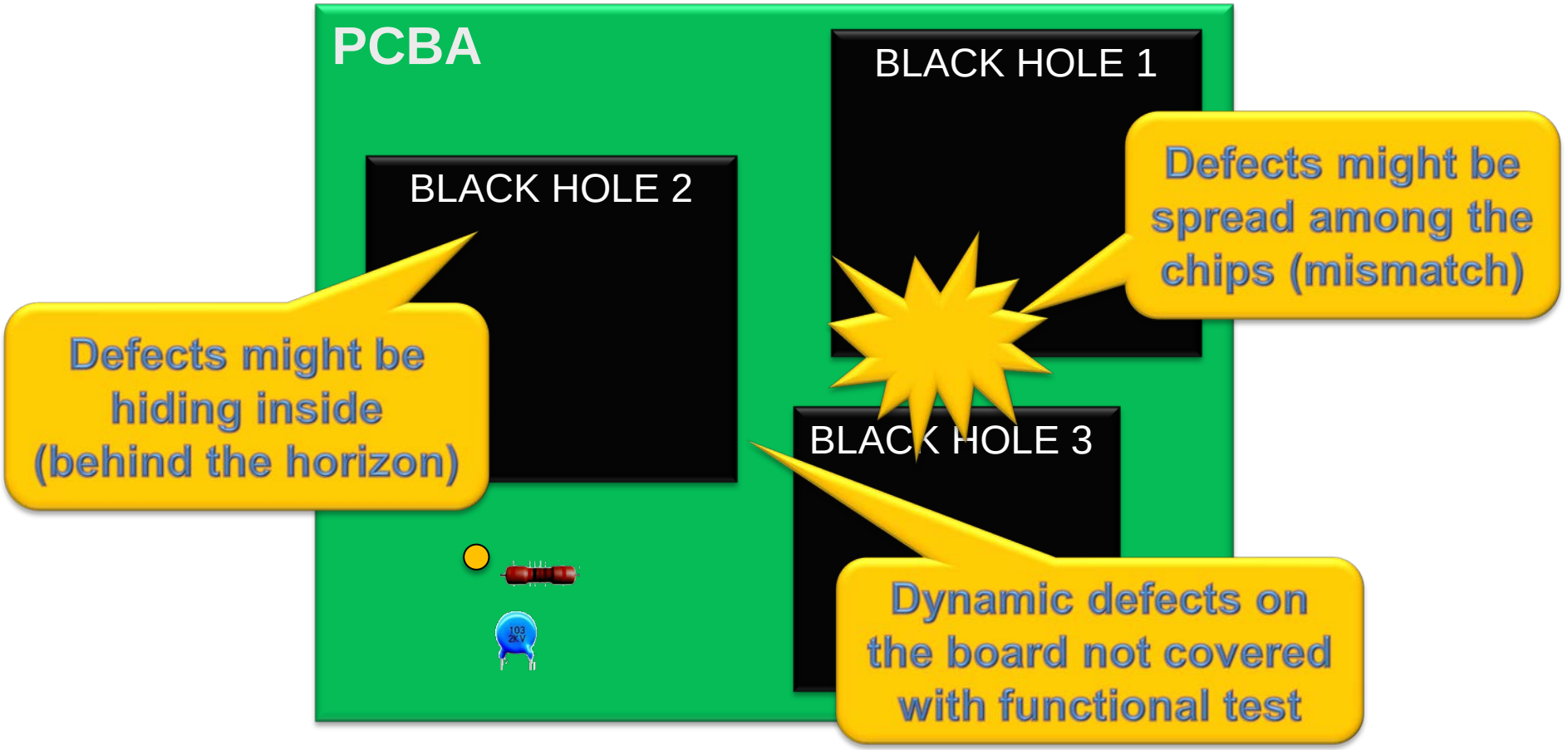


- 70% of all product returns characterized as NFF (US, 2008)
- an average family (in US) spends annually 65$ on NFF investigations

Testability Problem: good old days



Testability Problem: today



NO FAILURE FOUND?

NFF Cause – Dynamic Faults?

- Working Hypothesis
  - **Conclusion: quality of the existing tests is insufficient**
  - **Main hypothesis: good test methodology for dynamic faults is missing**

Test Method	Target Faults	Test Access	Diagnostics	Coverage
Structural	**Mainly static faults**	Scan test, JTAG, intrusive	Good	Good but **mainly static**
Functional	Dynamic	Functional code + external measurements	**No (pass/fail only)**	**Unknown**
Dream	**Dynamic**	**Non-intrusive**	**Good**	**Good (static + dynamic)**

Existing Test Coverage Metrics

Structural (Devices)	P	Presence
	C	Correctness
	O	Orientation
	L	Live BGA?
	A	Alignment
Structural (Connections)	S	Shorts
	O	Opens
	Q	Quality
Functional (Devices & Connections)	F	Feature
	A	At-Speed
	M	Measurement

- Good quality?
- Defect free?
- Within parametric tolerances?
- How to test?

Some metrics are **non-quantitative** => the test effectiveness is difficult to measure!

Good coverage of dynamic faults is missing?

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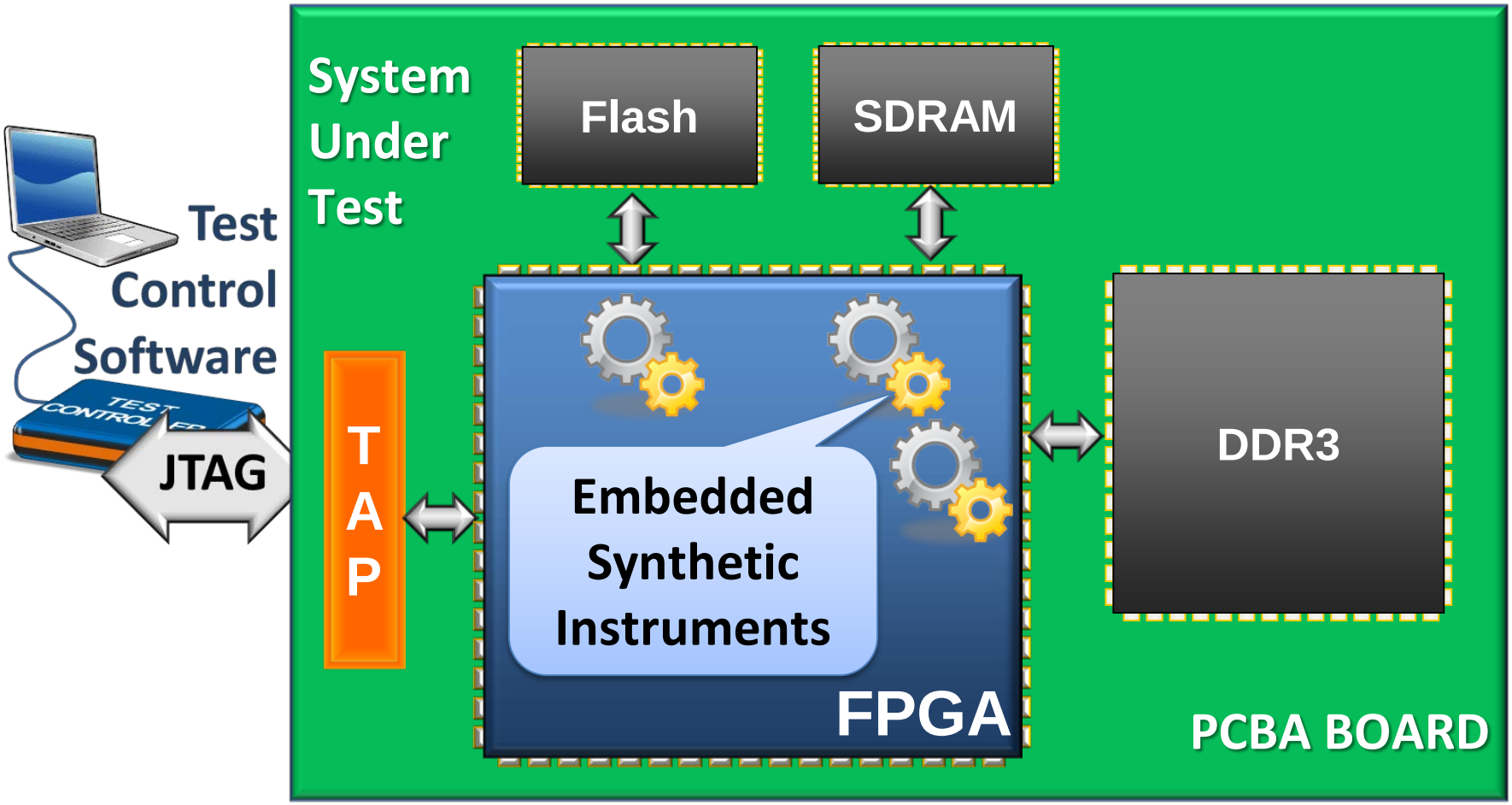
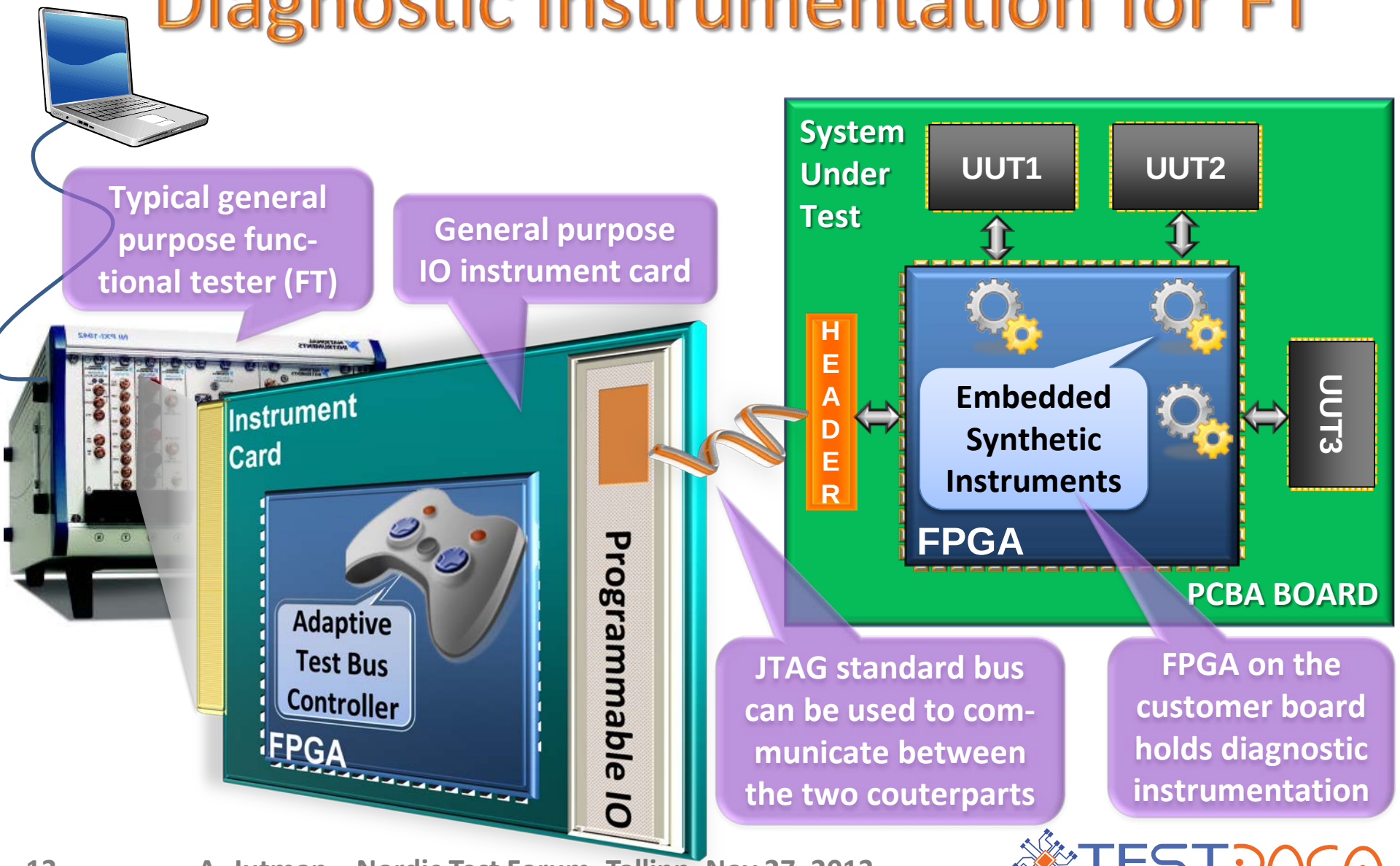
JTAG-controlled FPGA Instruments



Diagnostic Instrumentation for FT



Squeezing The Test Time

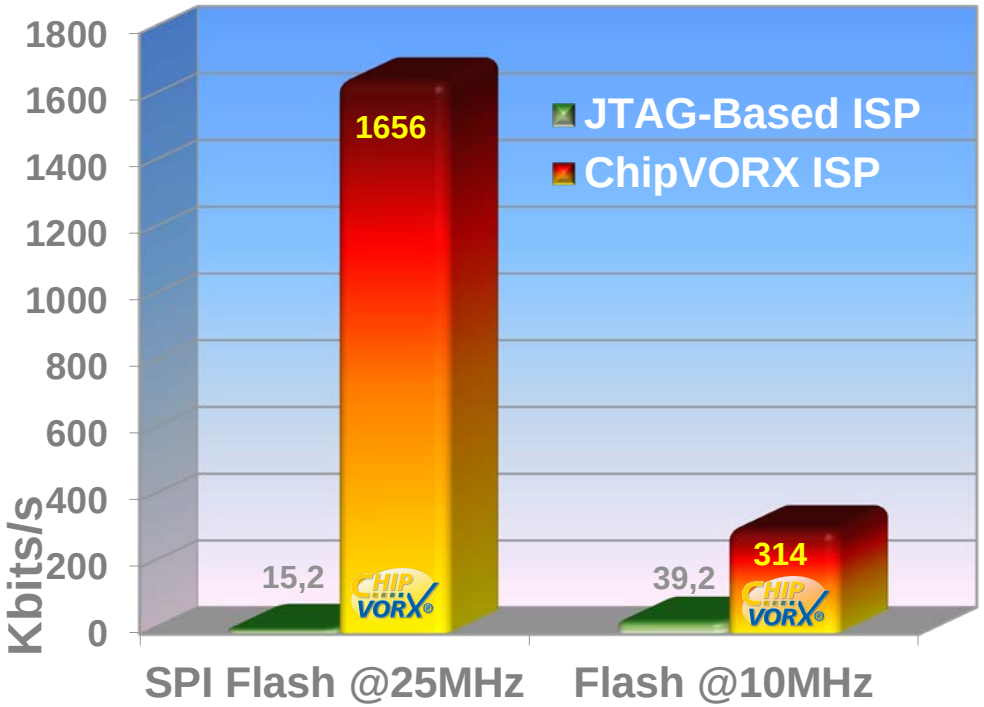
Typical JTAG test batch run time breakdown

Cluster Tests
RAM Tests
Infrastructure & Interconnect Tests

Accelerated test batch

ChipVORX accelerates the *most time-consuming* phases of the JTAG test batch

Data Throughput of Flash Programming (ISP)



	ICT	Flying Probe	Boundary Scan	Processor-based Test	Func-tional Test	FPGA instruments
DUT access	Fixed nails	“Flying” nails	Scan cells	mP core	mP / FPGA	**FPGA**
Test implementa-tion cost	High	Medium	Low	High	High	**Medium**
Structural Fault Coverage	Analog/ Digital	Analog/ Digital	Digital	Digital	Uncountable	**Digital**
Dynamic Fault Coverage	No	No	No	High	Uncountable	**High**
Test automation	High	High	High	Low	Low	**High**
Test scalability	Limited	Limited	High	Medium	Low	**Medium**
Test compatibility	High	High	High	Low	Low	**High**
Test access	Low	Low	High	High	High	**High**
Invasiveness	High	High	Low	Low	Low	**Low**

Benefits of Embedded Instruments

- Naturally integrated into the board design
  - No hardware changes required / no additional DFT structures
  - FPGA is typically connected to main system buses and is JTAG accessible
- Intended for PCB test beyond the FPGA itself
  - Unlike embedded into ASICs (e.g. BIST) which are used to test the IC itself
- Run as a part of system in operational mode
  - Instruments are capable for high-speed/at-speed/real-time test
  - Can natively support signaling protocol of target device
- Extremely flexible due to reconfigurable nature of FPGAs
  - Instruments are reconfigurable for meeting the requirements of particular PCB and test-case
- Reuse of IEEE1149.1 JTAG protocol
  - Compatible with existing test hardware (JTAG controllers)
  - Can be integrated with automatic Boundary Scan test flow

Embedded Synthetic Instruments

- Cover dynamic faults (at-speed test)
- Provide measurable quality (defect coverage)
- Good for diagnosis and troubleshooting
- Provide feedback for process tuning
- Non-intrusive
- Do not provide fit-for-function proof
- FPGA is needed on board

Embedded Synthetic Instrumentation improves the test quality

Defect Coverage Analysis

Structural (Devices)	P	Presence
	C	Correctness
	O	Orientation
	L	Live
	A	Alignment
Structural (Connections)	S	Shorts
	O	Opens
	Q	Quality
Functional (Devices & Connections)	F	Feature
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	M	Measurement

Instrumentation covers all except for Allignment and Feature

Exact Coverage is Still Unknown!

Structural (Devices)	P	Presence
	C	Correctness
	O	Orientation
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Further research is needed!

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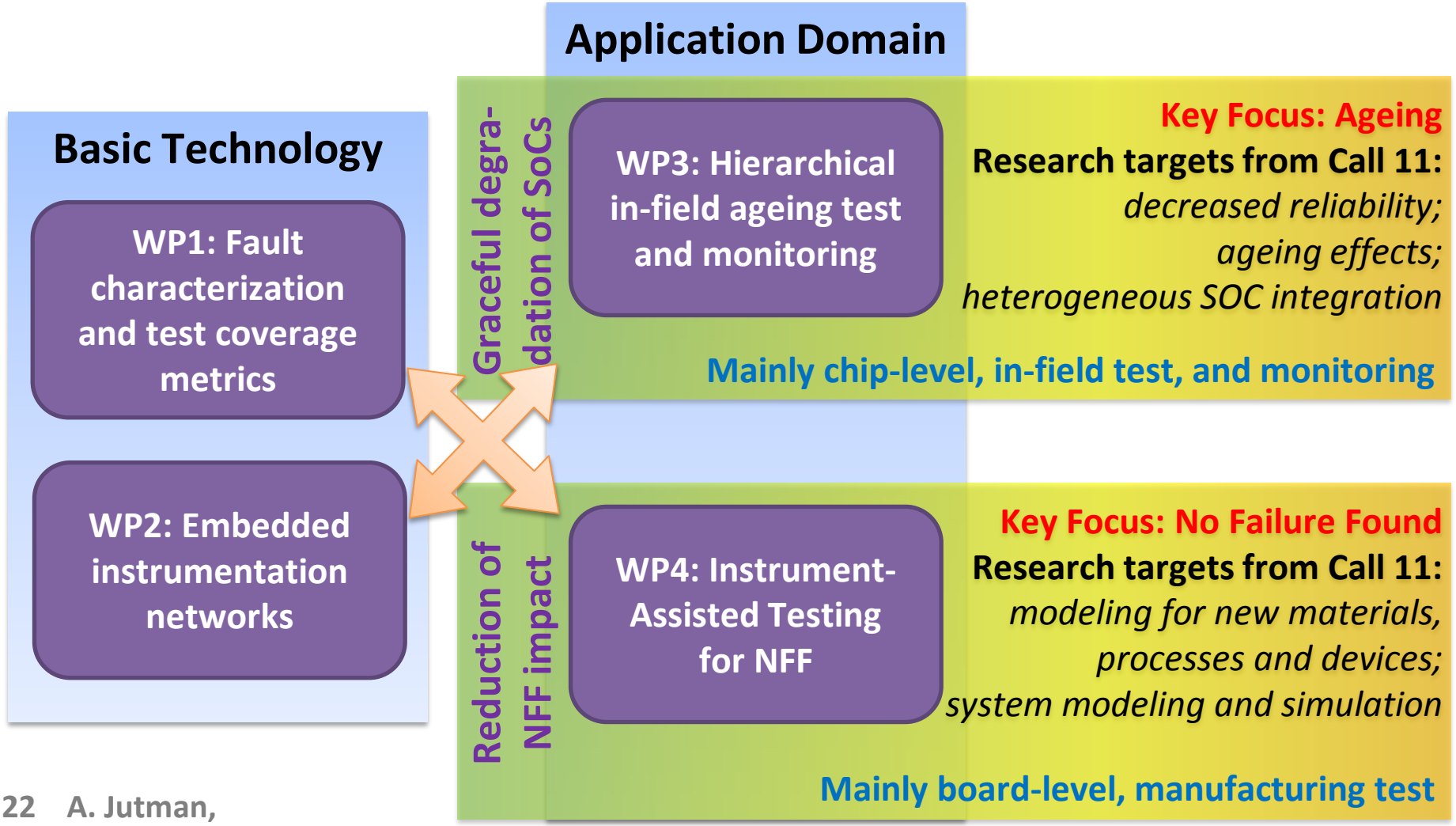
Focus Targets of FP7 BASTION

- The 2012 ITRS lists **ageing** (NBTI, PBTI, HCI, etc.) in semiconductor devices as one of the few most difficult challenges of process integration that affects reliability.

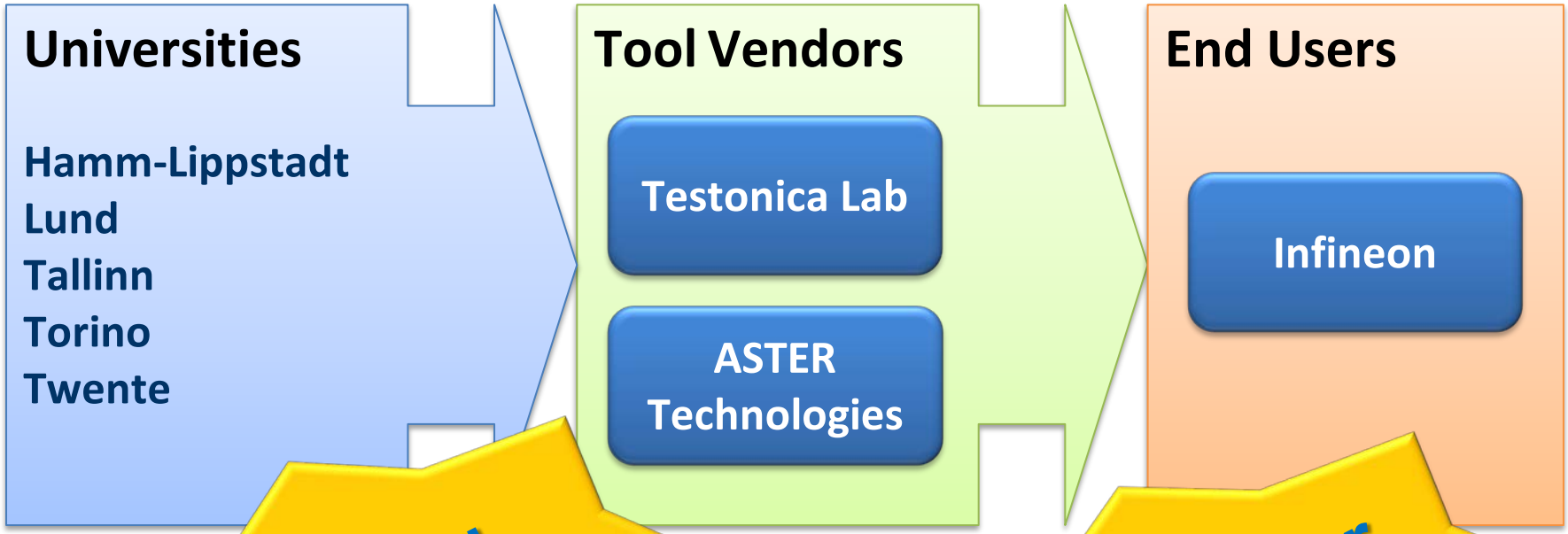
- **NFF** is being increasingly reported by industry and according to Accenture Report, in 2008 in US, around **70% of all product returns** were characterized as NFF. Cost-wise (including returns processing, scrap and liquidation), NFF amounted up to **50% of 13.8 billion USD** (10.5 billion EUR) returns and repairs cost in US.

FP7 BASTION: Research Targets & Expected Outcomes



FP7 BASTION Consortium Composition

Project results exploitation value chain



Starting January 2014

We look for assotiate partners!

TESTONICA
www.testonica.com

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Conclusions

- Growing importance of instrument concept in test application
- On-board FPGA can become an efficient embedded tester
- Systematic embedded instrumentation framework provides a scalable automated test solution
- The novel technology provides:
  - Significant speed-up in test application time
  - Improved test quality

BUT: further research is needed!

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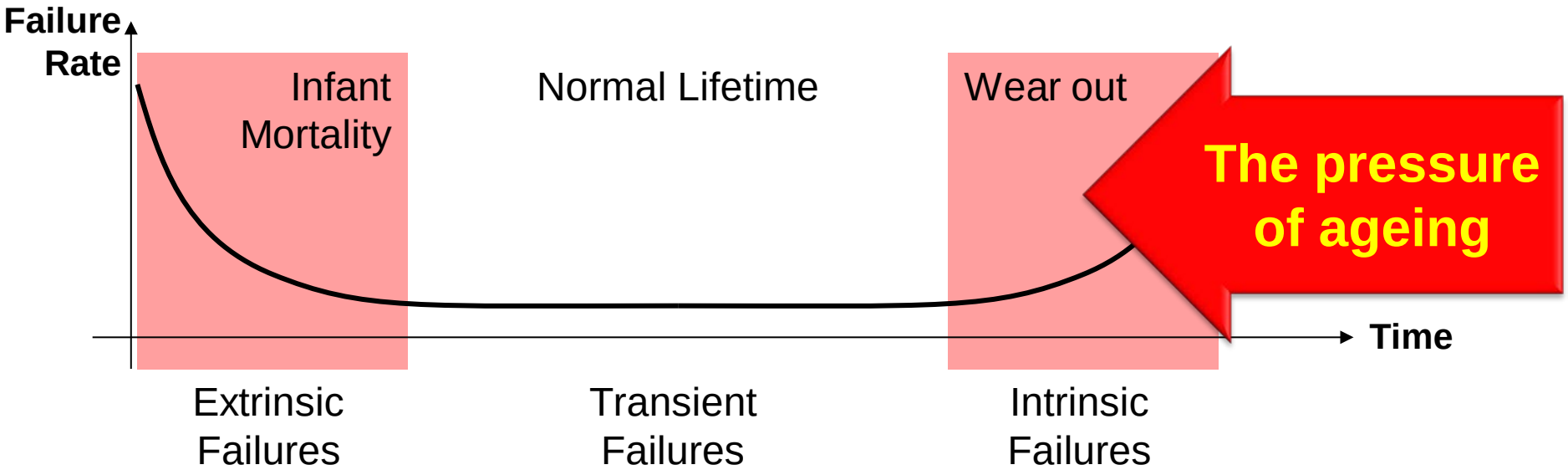
Failure Rates vs. Lifetime



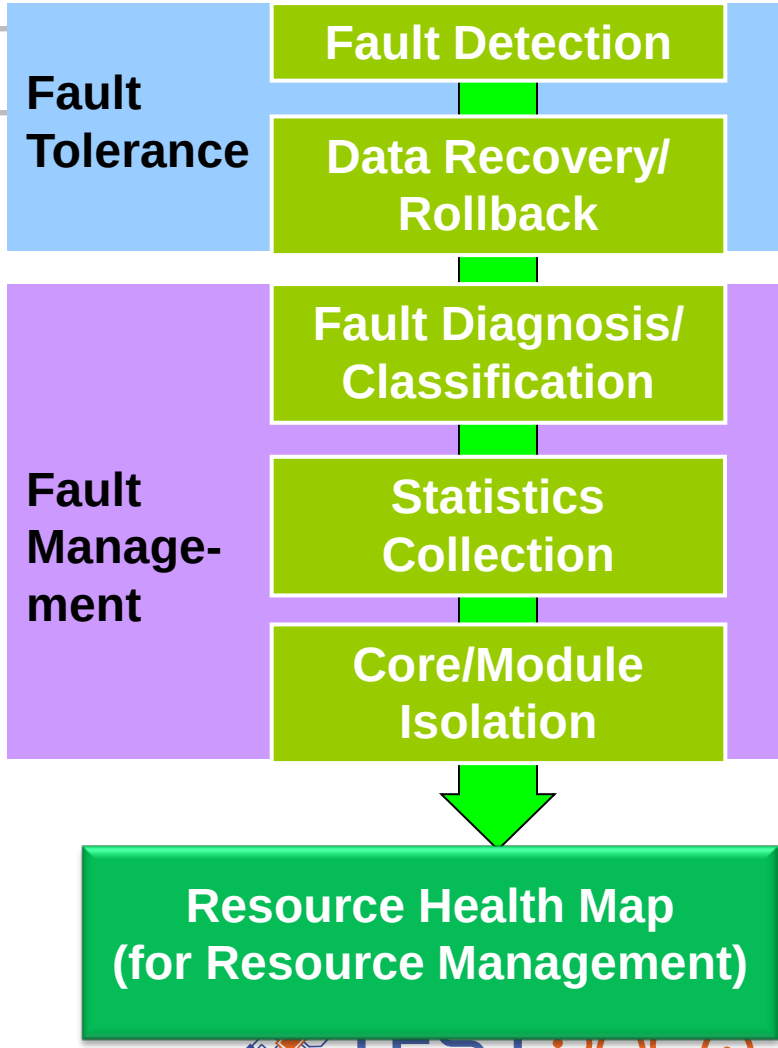
Solutions:

Testing	Fault Tolerance	Failure Resilience
Burn-in	TMR, ECC, parity	ECC, BIST, BISD
I_{DDQ}	BISER, Muller C element	Reconfiguration
BIST	Hardening	Adaptation, repair
ATE	Checkers	Spare components
Spare components	Signatures	

Fault Management: Going Beyond the Correction

Fault detection and recovery is NOT enough

- Fault Management provides co-operation between Fault Tolerance and Resource Management
- Diagnostic and statistical data is collected
- Classification of failures is done
  - Fault type: transient / permanent
  - Fault granularity: module / IP core
  - Criticality
- System health map is maintained



Requirements for an Efficient FM System

- Has to be **simple** and reliable
- **Independent** from normal system functionality
- Has to be operational when system itself is not functioning properly
- Non-intrusive during normal operation
- **Scalable** and systematic
- Provide **immediate reaction** on errors
- Provide rollback and recovery (task rescheduling)
- Diagnose and **classify faults** as a background process
- Maintain **system health** information

Why IEEE P1687 ?

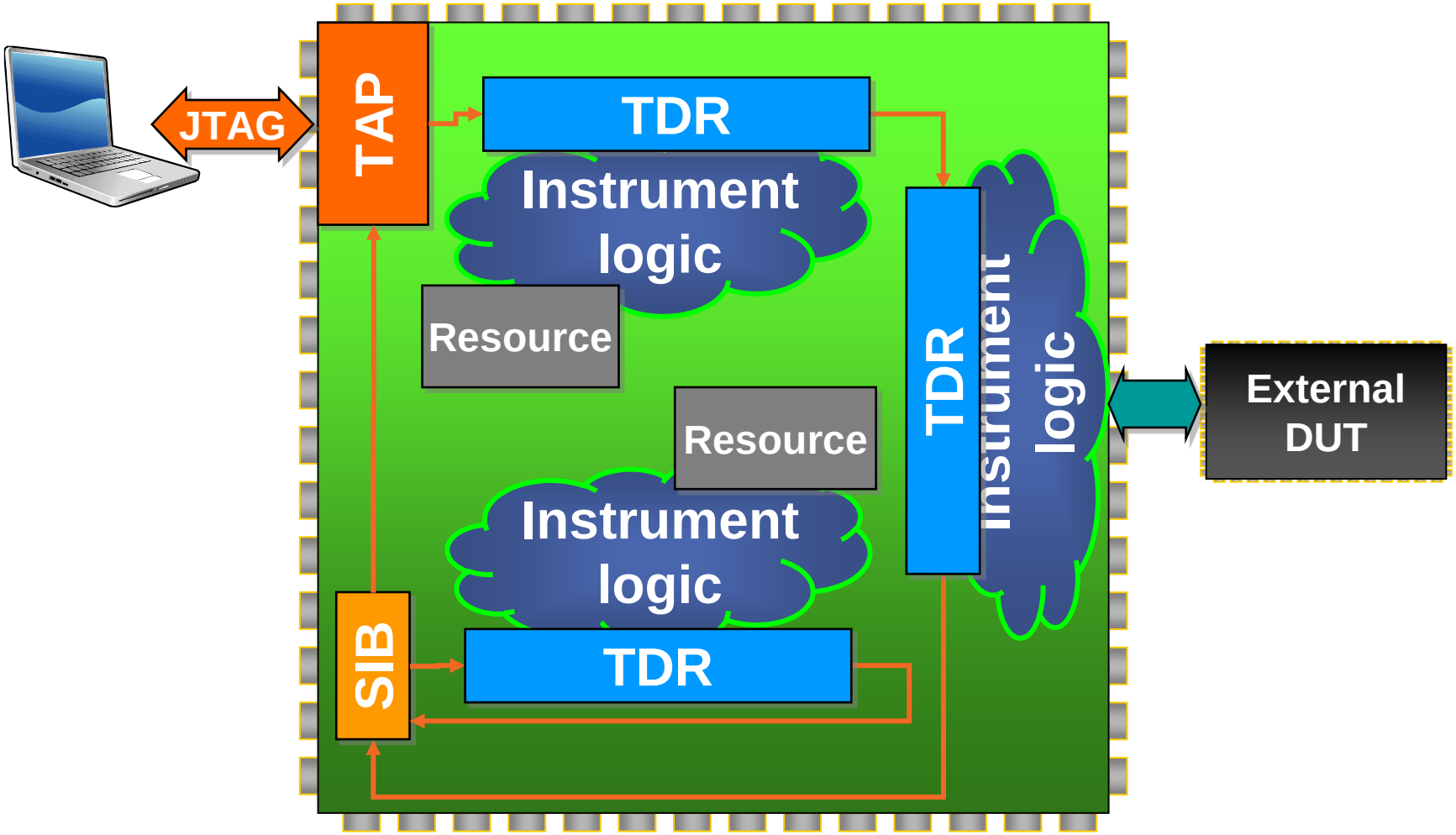
IEEE P1687 - Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

STANDARD

=

AUTOMATION

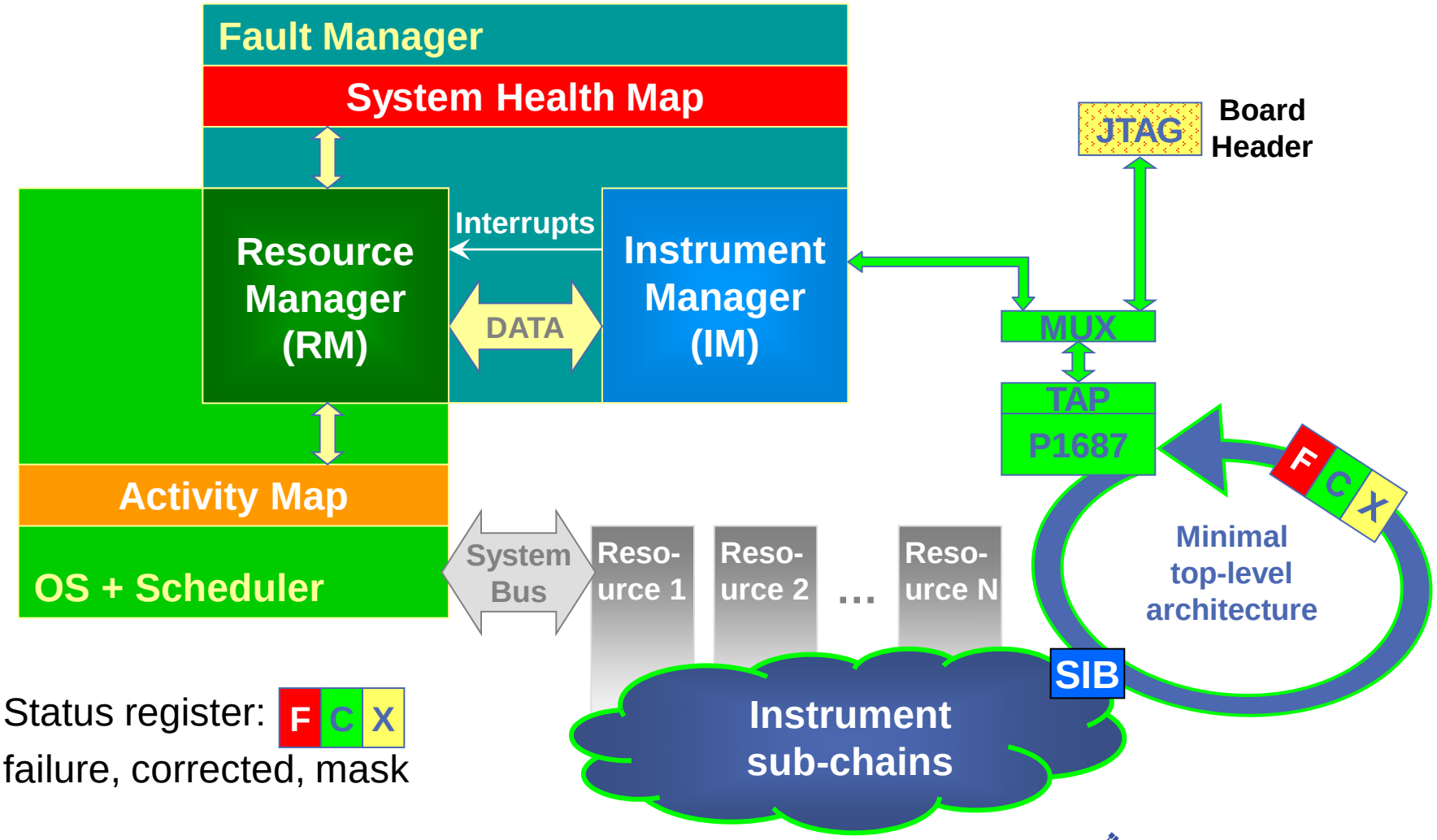
IEEE P1687/IJTAG Infrastructure



Objectives

- **Integrate** all DFR structures into a single service infrastructure
- Provide seamless integration possibility for IP cores from **different vendors**
- Fault Management infrastructure should be **independent** from the rest
- Take benefit of **embedded instruments** and corresponded standard IEEE P1687

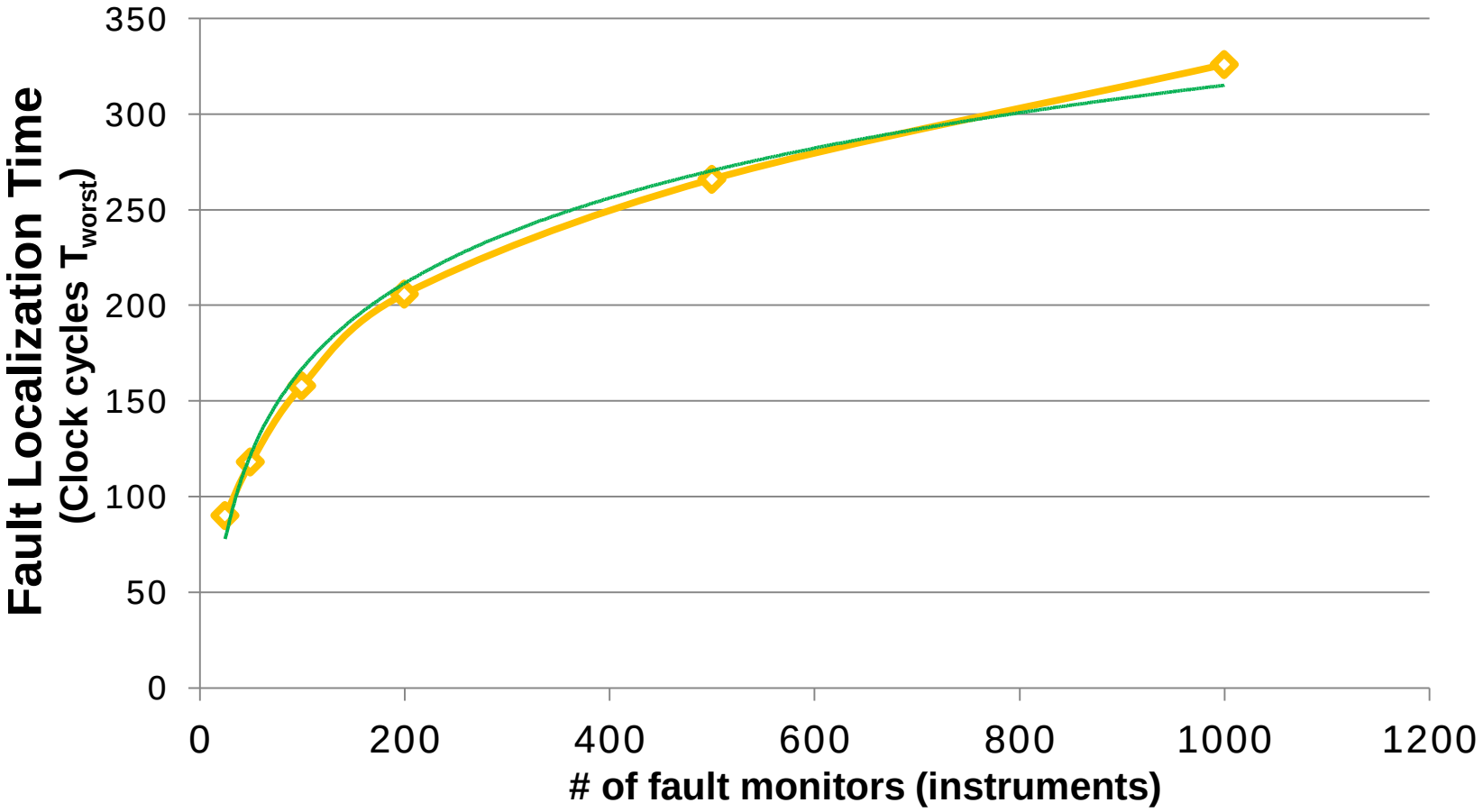
Fault Management Infrastructure



Status register: F C X

failure, corrected, mask

Logarithmic Scaling of the Latency



FP7 BASTION: Summary of Topics

- **No Failure Found** and Test Coverage Metrics
- IEEE P1687 assisted Fault Management against **Ageing Faults**
- Reuse of **embedded instrumentation** at the system/board level
- Instrument-assisted functional test