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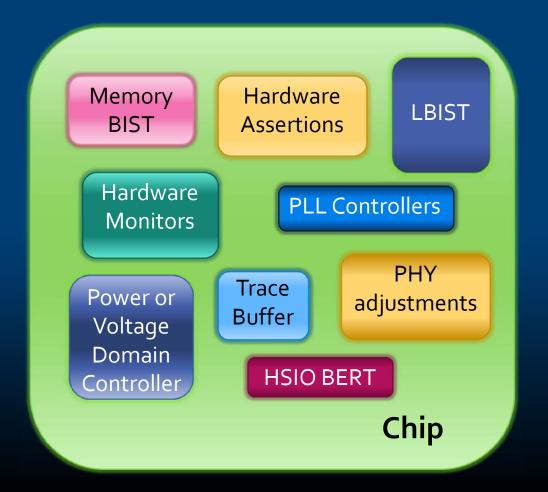


SECURING YOUR SYSTEM WITH P1687

Presented to the 2013 Nordic Test Forum

Motivation: On-Chip Instruments Need Access Protection

- Chips may contain multiple cores and hundreds of instruments
- Depending on the design, many of these can often be accessed through scan chains



On-Chip Data Also Needs Protection from Unauthorized Access

- Chip IDs
- Encryption Keys
- DVD codes
- Intermediate Execution States
- On-chip IP accessible through scan chain We need a way to prevent unauthorized users from accessing this information through the scan chain.

So, how can we protect things that must not be accessed?

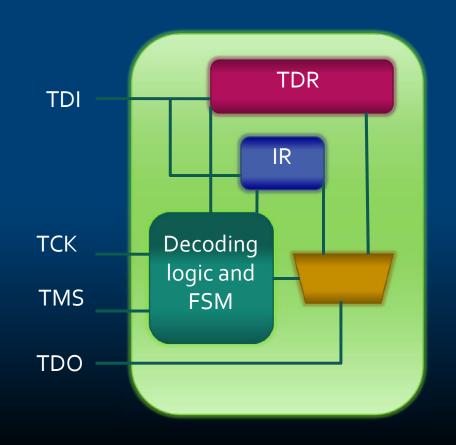
It depends on how you normally intend to access them in the first place.

Outline

- Protecting Standard JTAG
- Overview of P1687
- Hiding Instruments behind LSIBs
- Adding Traps for Extra Protection
- Distributing Locks, Keys, and Traps across
 Multiple Levels of Hierarchy
- Conclusions & Future Work

Internals of chip/board can be accessed with IEEE 1149.1

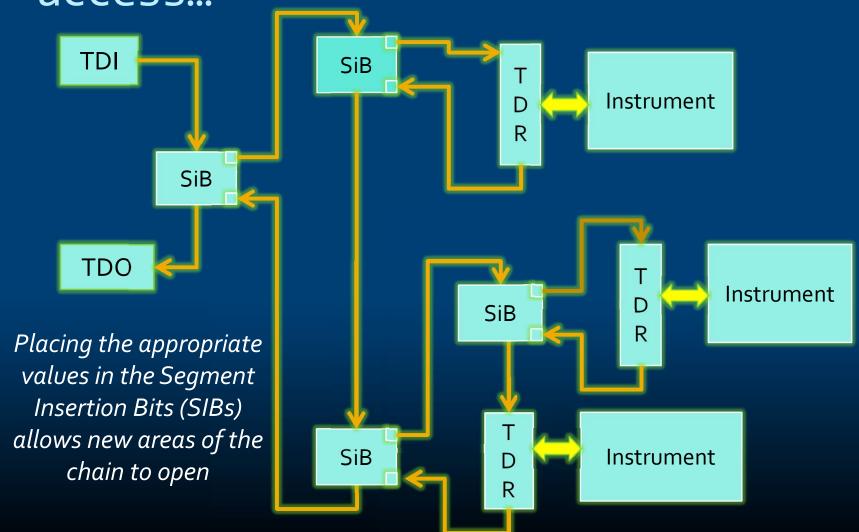
- Attackers can hack the JTAG port
 - Modify firmware (Xbox Hack)
 - Search for "private" instructions that are hidden test and debug features
 - Altera lists private instructions to avoid or you will destroy the chip!



How can information be protected in 1149.1?

- Burn out the JTAG port by fusing off the TMS signal.
 - Problem: Can no longer use JTAG for debug or field test.
- Others suggest adding extra hardware to handle challenge/response pairs
 - SHA256 HASH engine used to compute a hash with a secret key. (Clark 2010)
 - Random challenge generated with multiple ring oscillators
 - User must compute same hash
 - Security Authentication Module (SAM) and Access Monitor (AM). (Pierce 2011, 2012)
 - SAM locks JTAG interface on bootup and authentication protocol is used to unlock access and assess privilege level.
 - UpdateDR is blocked if user doesn't have privileges

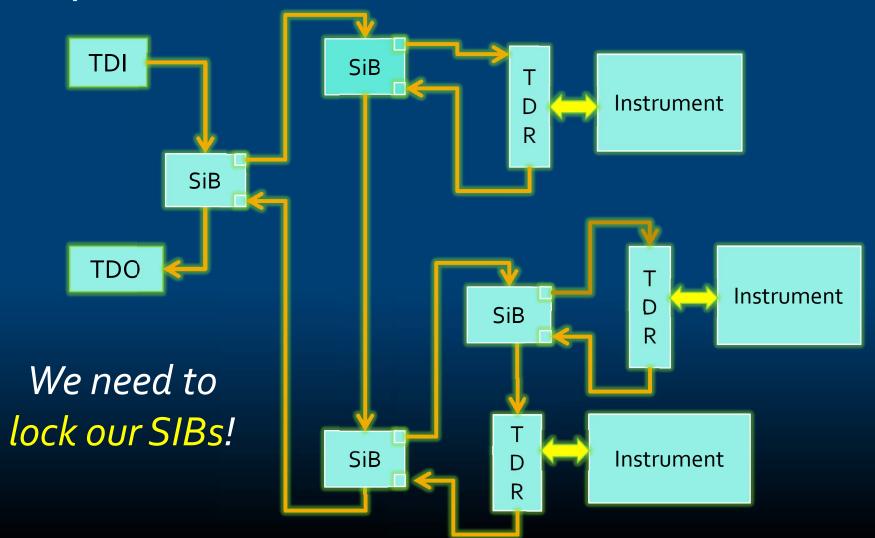
P1687 is designed for instrument access...



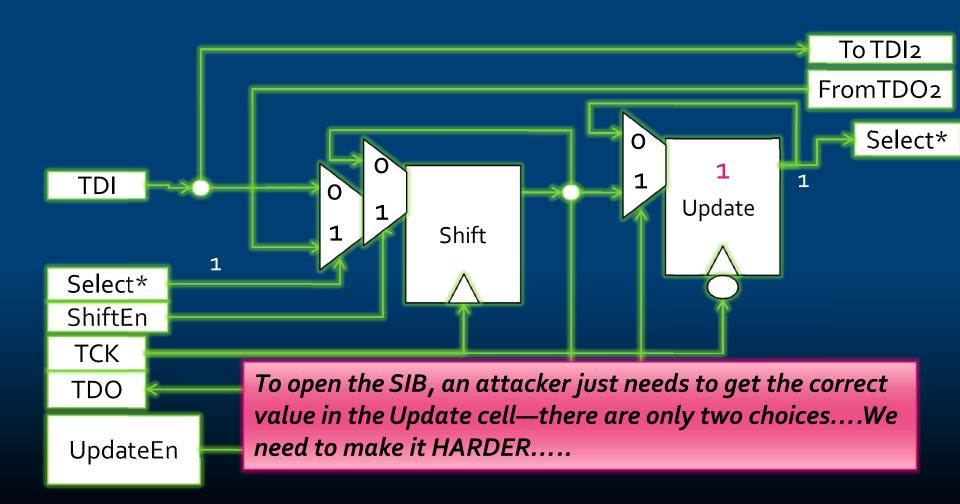
Can we harness the design of a P1687 network to inexpensively increase security by hiding instruments?

Yes!

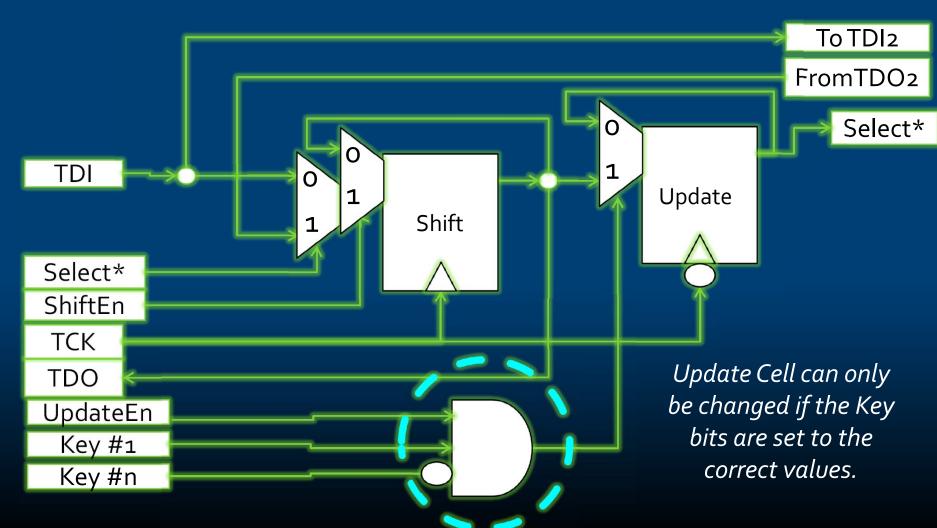
SIBs serve as doors that must be opened for instrument access...



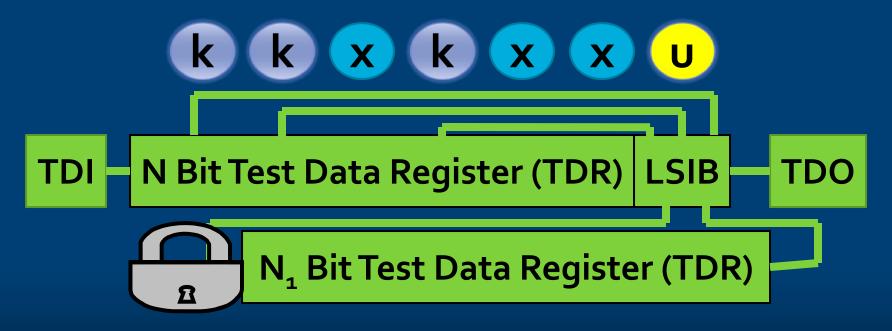
What does a normal SIB look like?



One Implementation of a Locking Segment Insertion Bit (LSIB)



The attacker must guess the right key bit values to open the LSIB...



If the attacker doesn't know anything about the network, he can start by trying random guesses....

How long is guessing likely to take?

How will the attacker know that a LSIB has been opened?

The Scan Chain Length generally changes when we open a SIB.....

How will the attacker know the length of the chain?

is recognized.

N-bit chain initially full of unknown data Start shifting in a distinctive **00101**XXXXX......XXXXXXXXXXX .01 d-bit pattern... After n-cycles, the pattern RRRRRRRRRRRRRRR.......**0100101** ... RRRR will be at TDO. After n+d cycles, pattern RRRRR ..0100101

How does the attacker make a guess?

The attacker uses the 1149.1 state machine to try to open the SIB

Update DR

Once a random vector is in the chain, Update DR needed to try to open LSIB: 1 cycle.

Run Test Idle

1 cycle.

Select DR

1 cycle.

Total time for a guess... 5+n+d

Capture DR

1 cycle.

Shift DR

1 cycle.

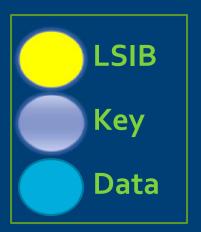
Shift Cycles

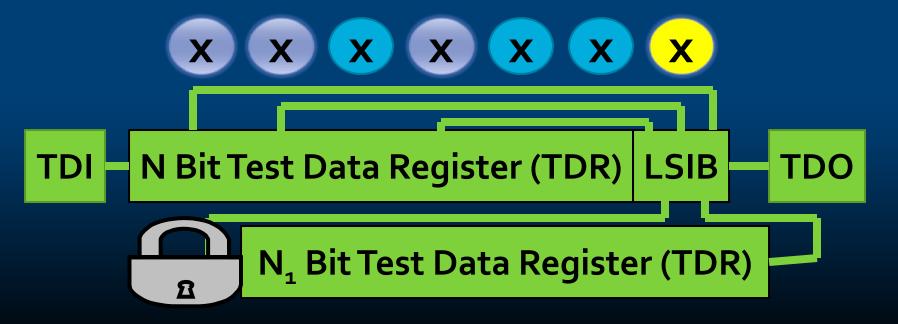
N+d cycles to check the length of the chain and shift in random bits.

Needed Key = 101

First guess = 1000010

Distinguishing seq = 0100101



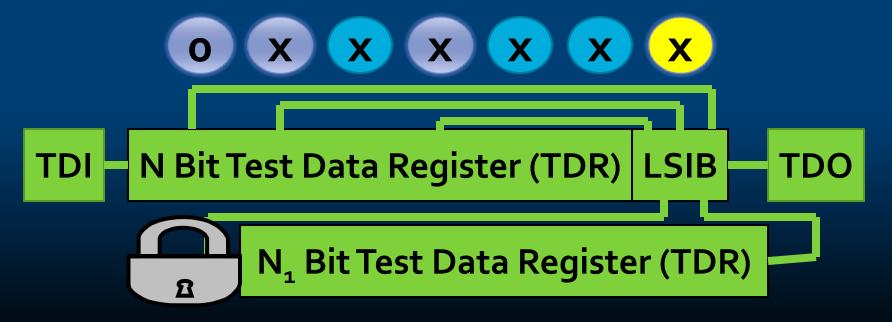


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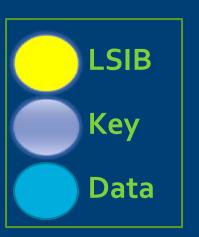


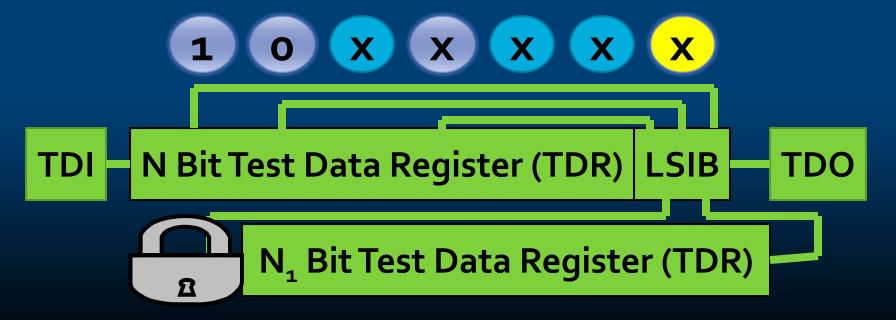


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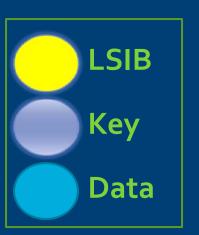


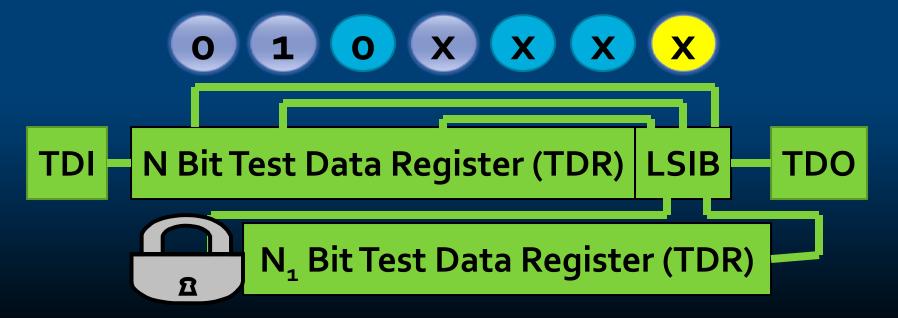


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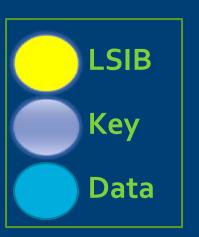


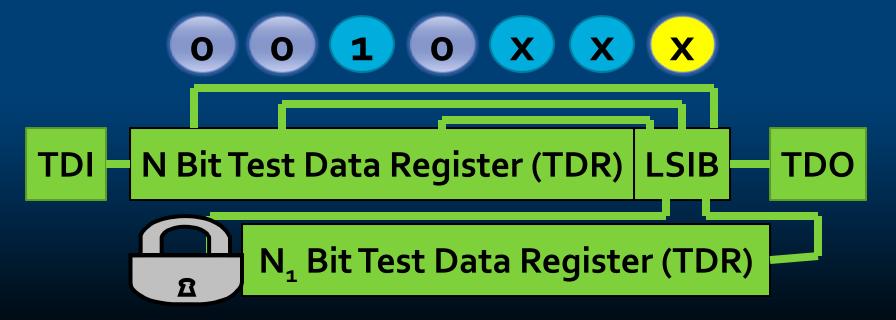


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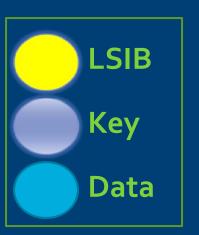


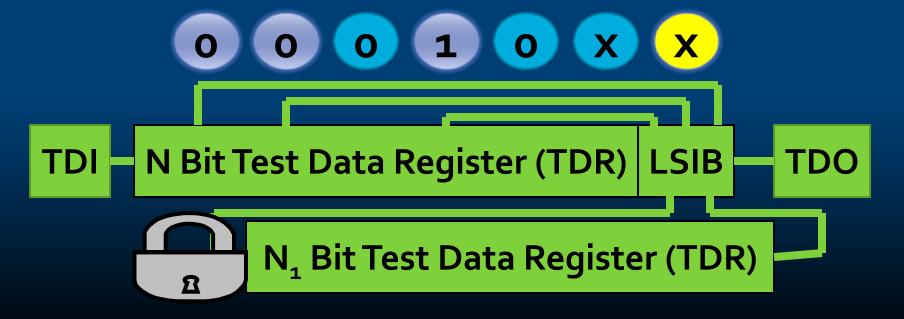


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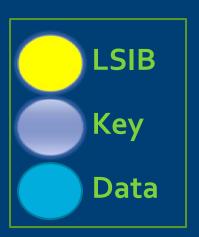


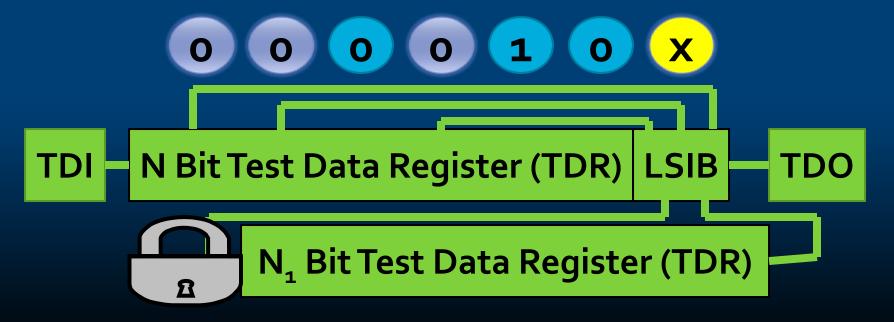


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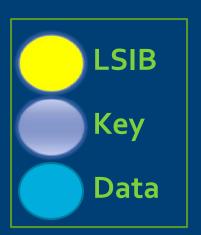


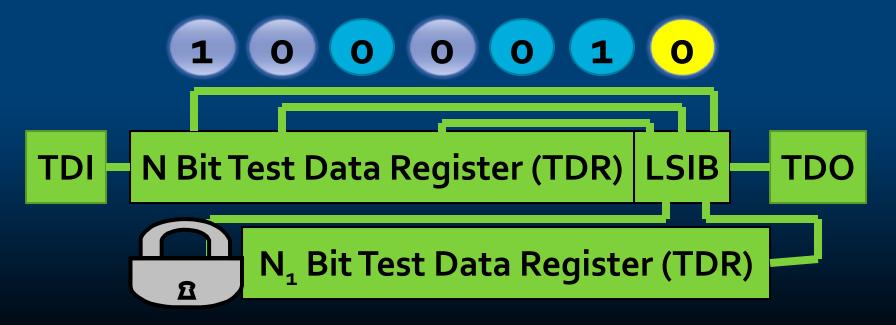


Needed Key = 101

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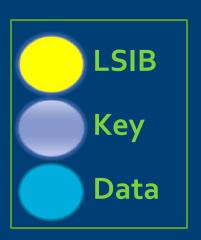


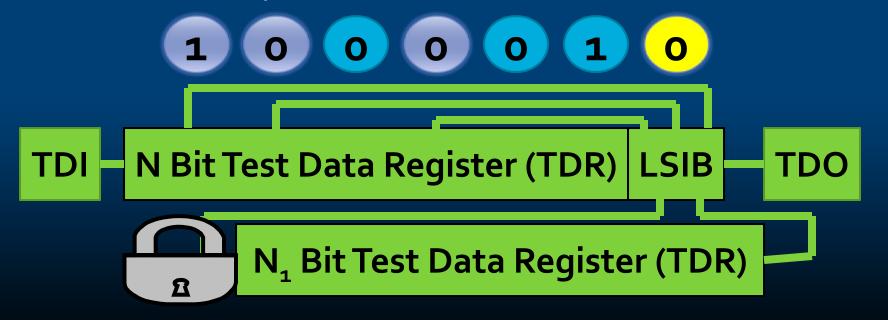
Needed Key = 101

First guess = 1000010

Distinguishing seq = 0100101

Perform UpdateDR.....it's still locked but we don't know that yet.



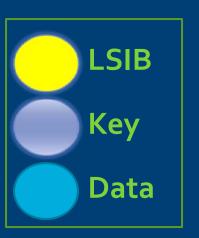


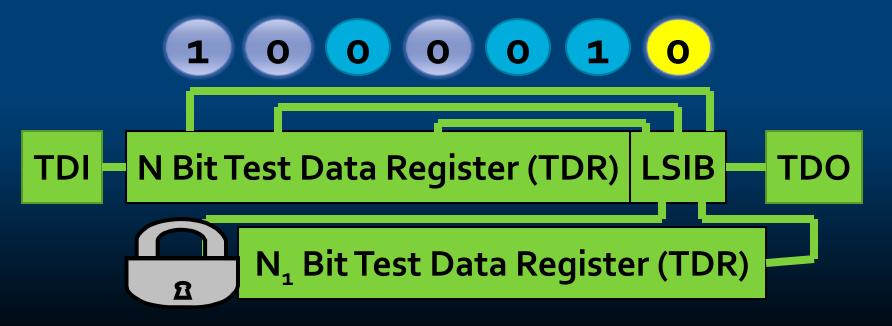
Needed Key = 101

First guess = **1000010**

Distinguishing seq = 0100101

Go through RunTestIdle and Select DR



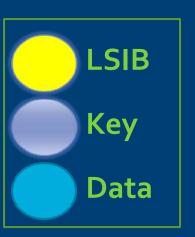


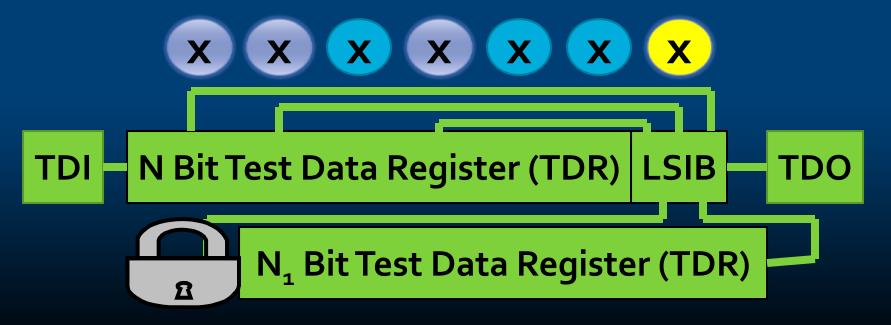
Needed Key = 101

First guess = **1000010**

Distinguishing seq = 0100101

Go through CaptureDR & ShiftDR

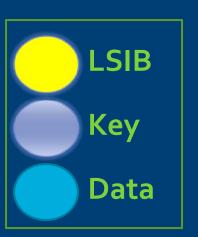


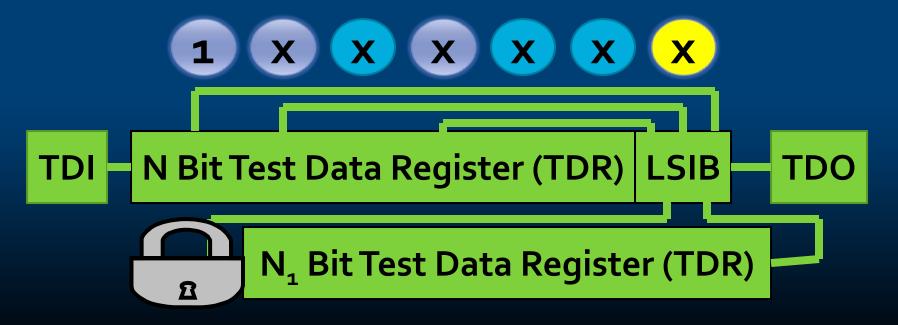


Needed Key = 101

First guess = 1000010

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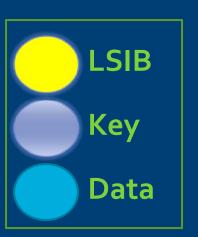


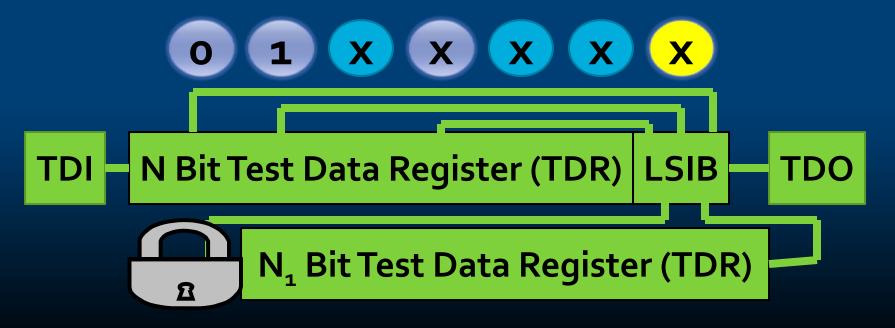


Needed Key = 101

First guess = **1000010**

Distinguishing seq = 0100101

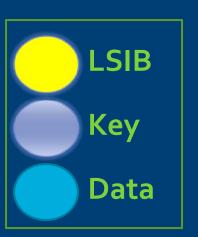


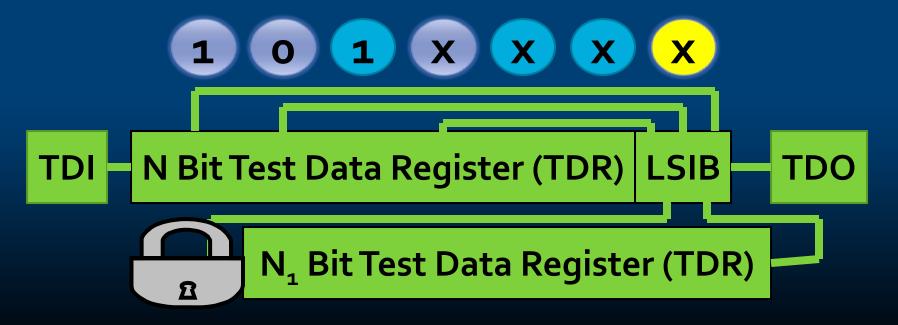


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First guess = 1000010

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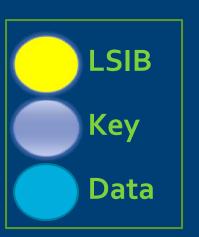


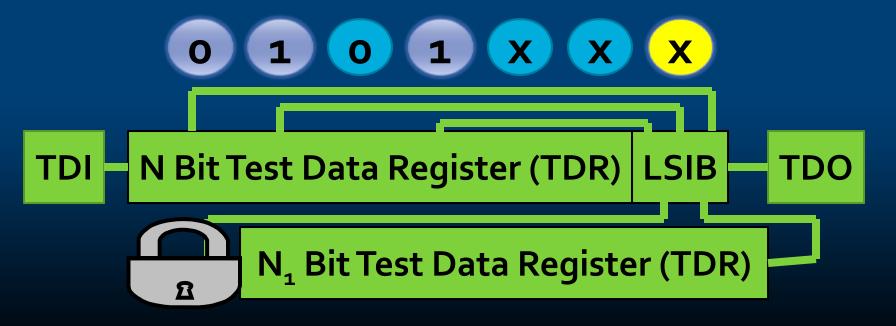


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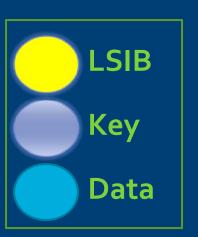


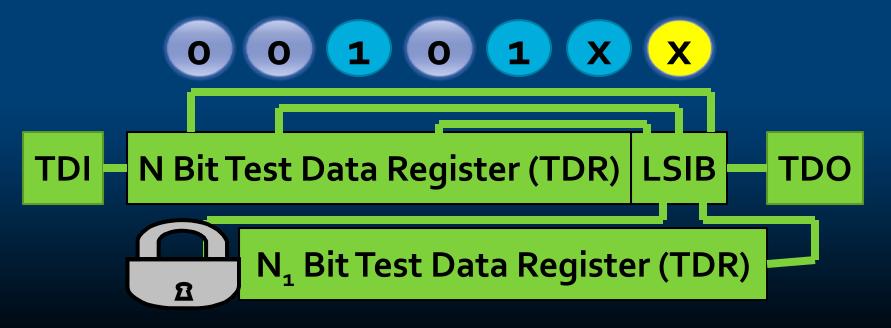


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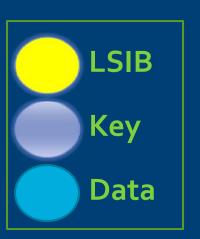


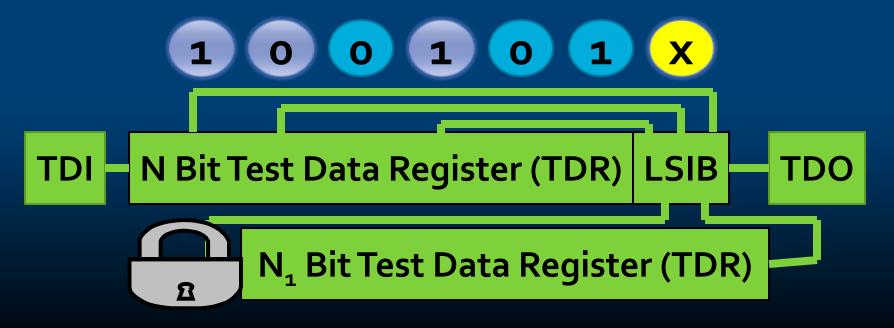


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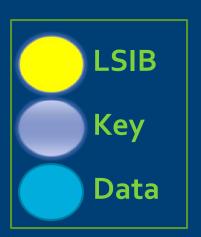


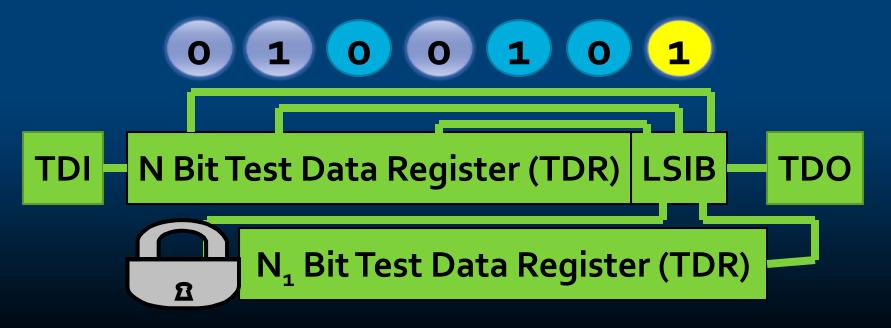


Needed Key = 101

First guess = 1000010

Distinguishing seq = 0100101





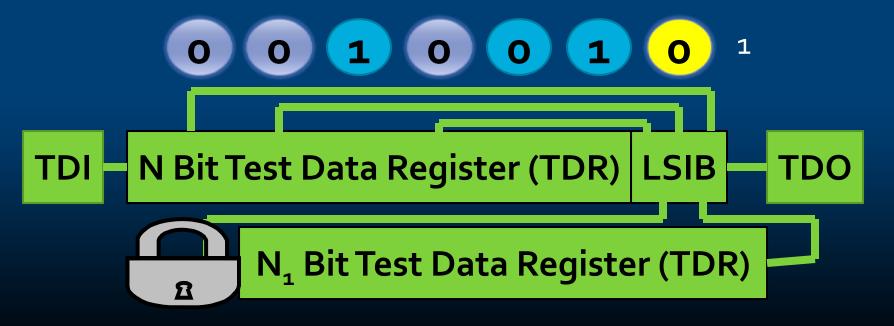
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Start shifting in second guess





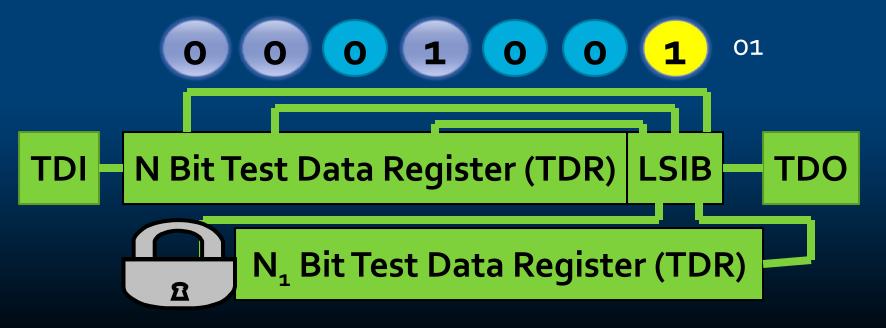
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Start shifting in second guess





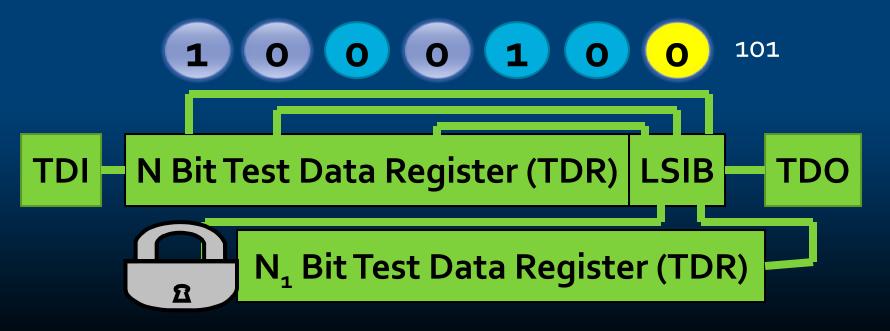
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Start shifting in second guess



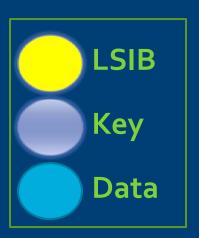


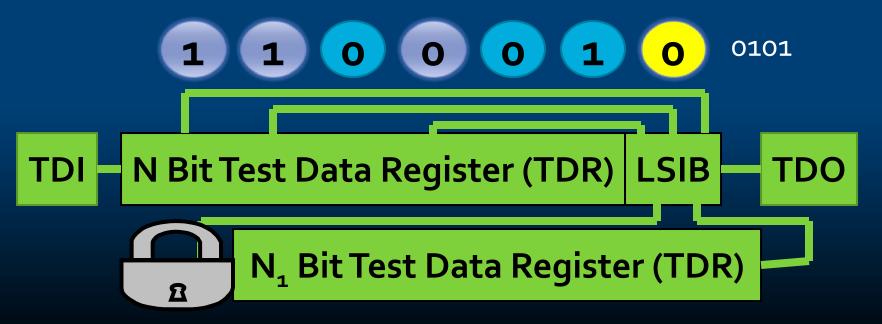
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Start shifting in second guess





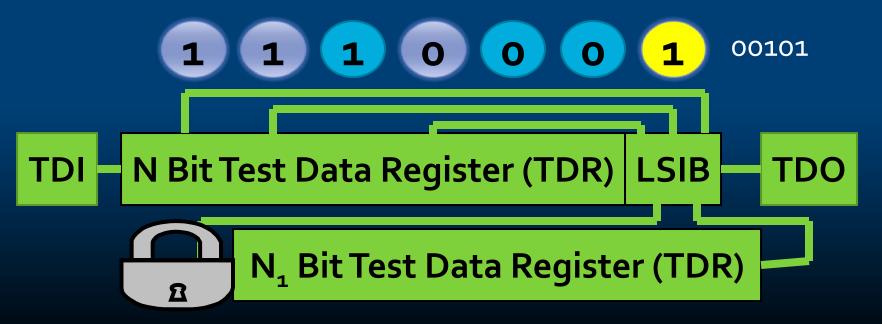
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Start shifting in second guess



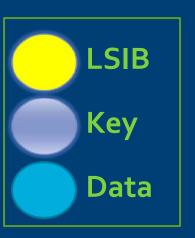


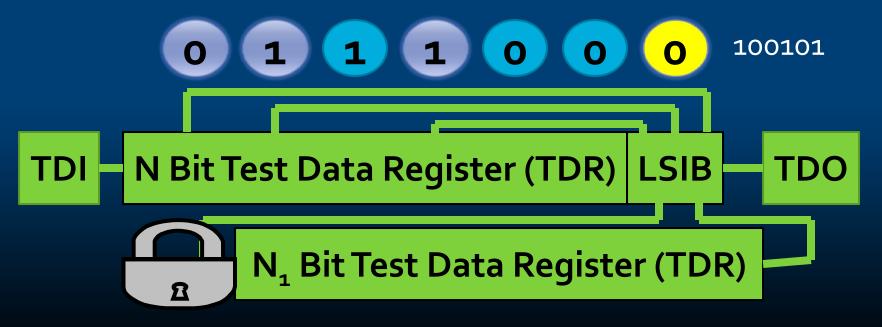
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Start shifting in second guess



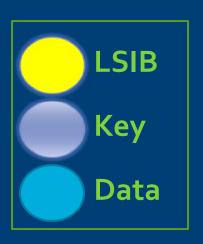


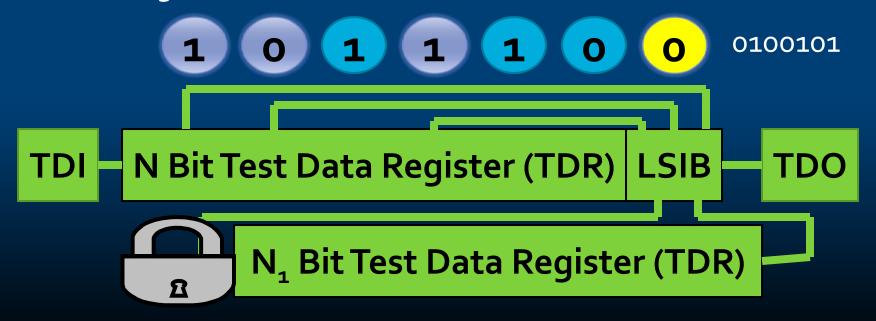
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Distinguishing seq = 0100101

Distinguishing sequence out when expected... Second guess is in chain....



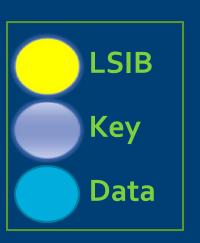


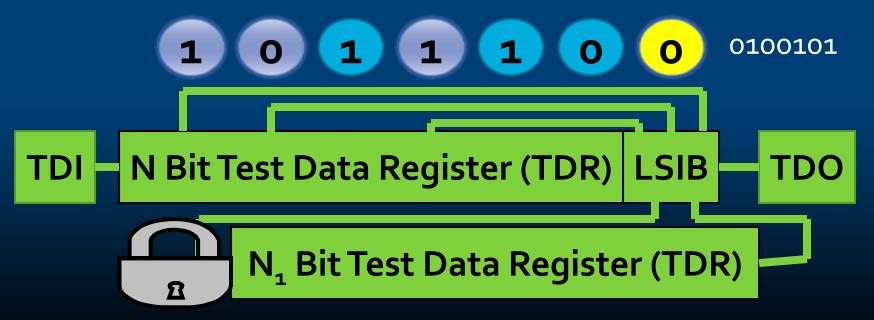
Needed Key = 101

Second guess = 1011100

Distinguishing seq = 0100101

Pull UpdateDR....Key is right, but wrong value in LSIB....Still locked....





How long until the attacker successful?

- Number of possible combinations for k bits in the key and 1 value LSIB = 2^(k+1)
- Probability of guessing the correct combination = $1/2^{(k+1)}$
- Expected number of tries before the correct guess is selected = 2^(k+1)
- Cost of a guess = 5+n+d clock cycles
- Total expected clock cycles to open LSIB with random guesses = (5+n+d) *2^(k+1)

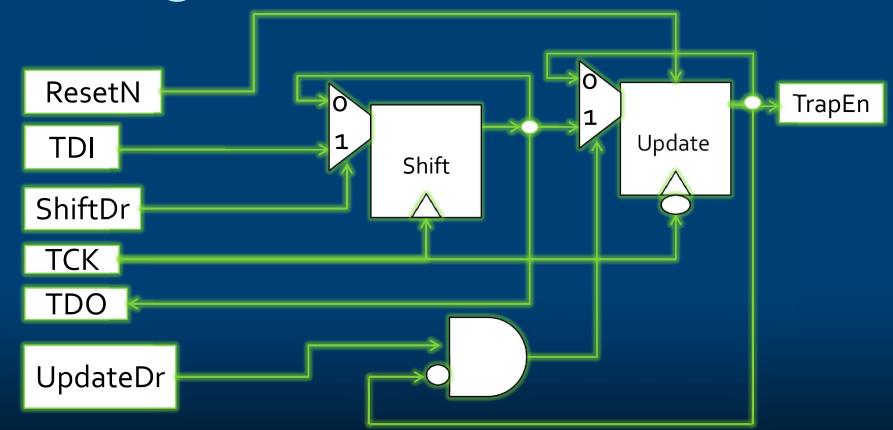
How long does it take to open an LSIB (assuming shifting at 10 MHz & d=25)?



Of course, an attacker could be lucky...and guess correctly on the first couple of tries...can we make it harder?

Yes!!! We can set traps and use hierarchical LSIBs architectures....

TRAPs—Once you fall in, you can't get out...



- •Trap is sprung if the wrong value (1) present on an updateDR
- •TrapEn can keep an LSIB from opening or a key-bit from updating
- Can be designed to only reset on global or local reset

How does the attacker make a guess with TRAPs present?

Disable Traps: Reset Update DR needed to try 1 cycle. Update DR to open LSIB: 1 cycle. Depends on RESET Reload IR Behavior and IR size. Run Test Idle 1 cycle. 1 cycle. Run Test Idle 1 cycle. Select DR 1 cycle. Select DR 1 cycle. Capture DR 1 cycle. Capture DR 1 cycle. Shift DR 1 cycle. Shift DR N+d cycles to check **Shift Cycles** New pattern of chain length. shifted in: N **Shift Cycles** cycles

How does the attacker make a guess with TRAPs present?

Disable Traps: Reset Update DR needed to try 1 cycle. Update DR to open LSIB: 1 cycle. Depends on RESET Reload IR Behavior and IR size. Run Test Idle 1 cycle. Cost of a guess if attacker thinks Traps Select DR may be Present: $\geq 10 + 2n + d$ 1 cycle. Capture DR Capture DR 1 cycle. 1 cycle. Shift DR 1 cycle. Shift DR N+d cycles to check **Shift Cycles** New pattern of chain length. shifted in: N **Shift Cycles** cycles

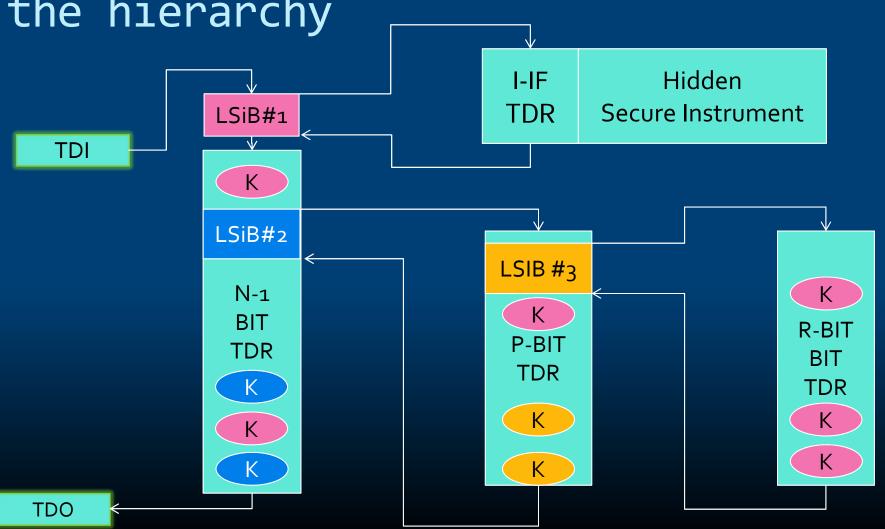
How long does it take to open an LSIB with traps?

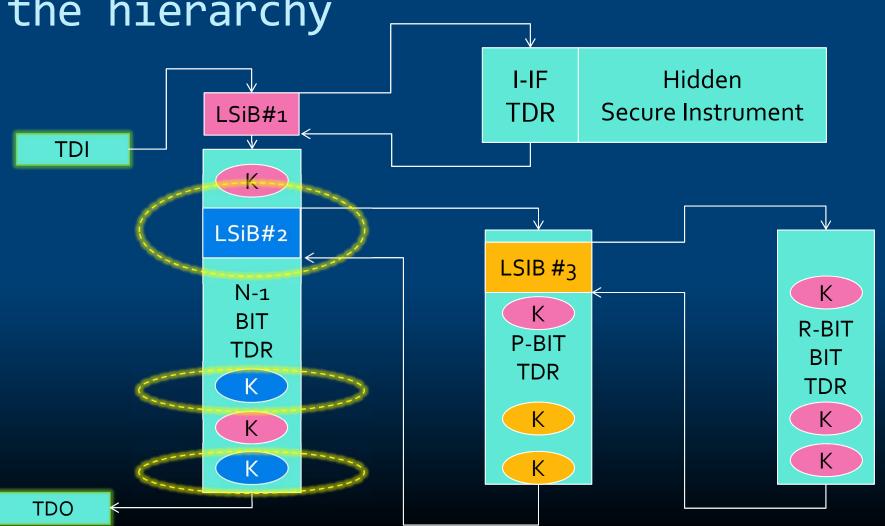


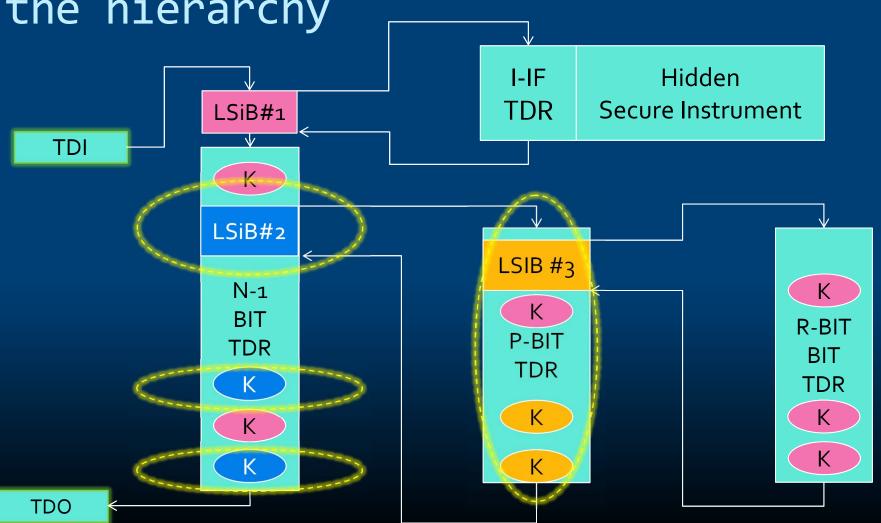
K=number of key bits, N=number of bits in chain

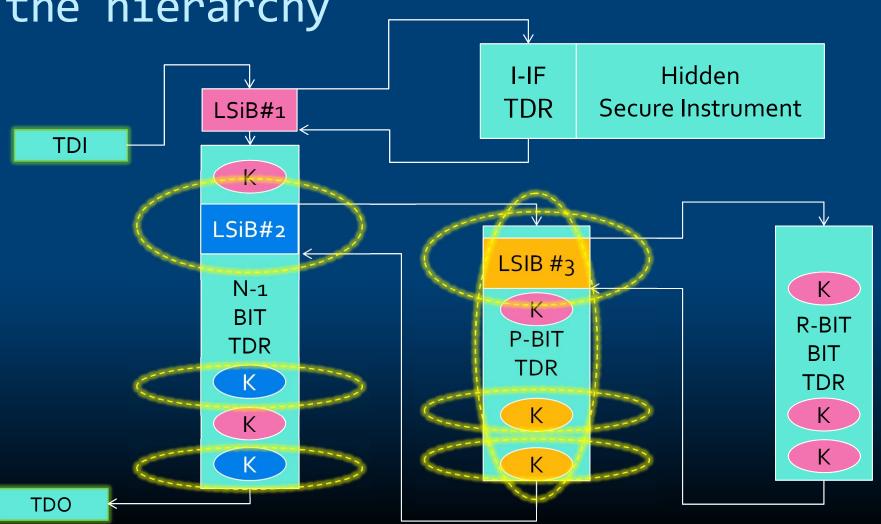
But...couldn't they still get lucky and guess right the first time?

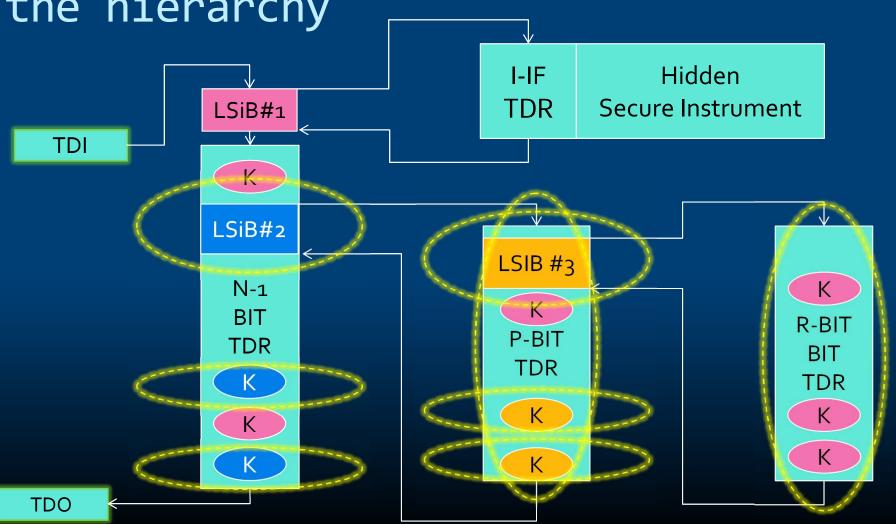
Yes...but what if they have to be lucky and guess right multiple times?

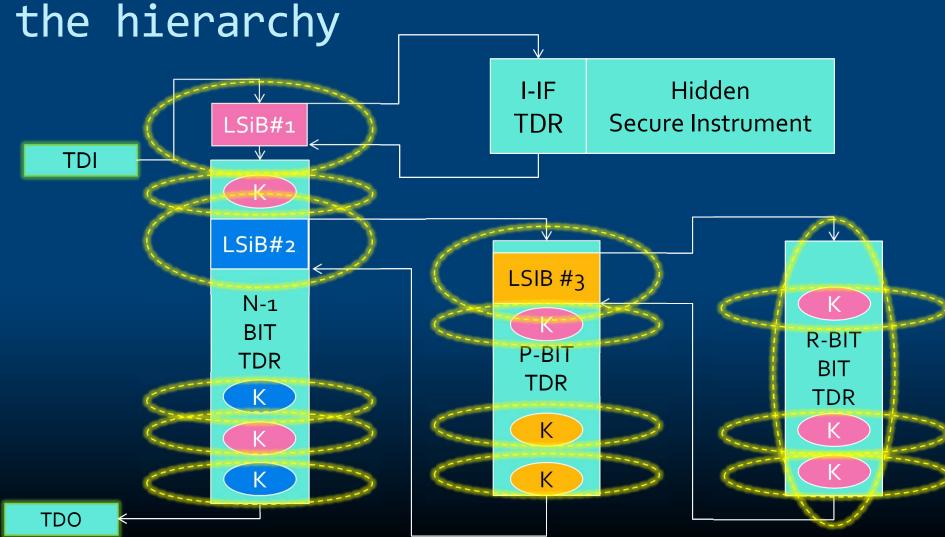


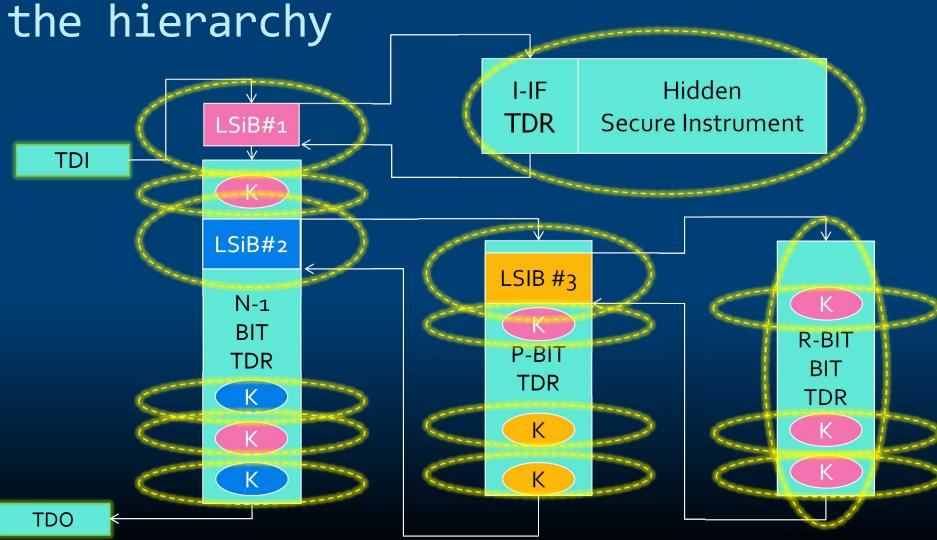








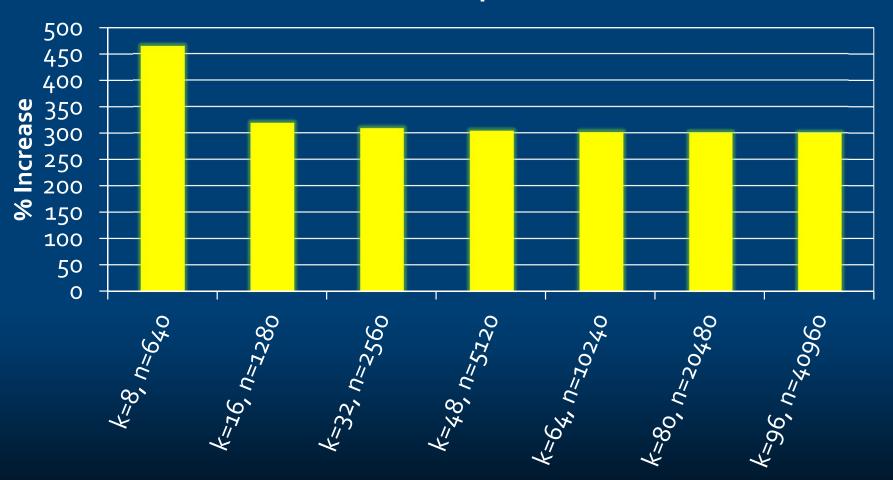




Hierarchical Structure Increases Time for Access

- Multiple LSiBs may need to be unlocked in a particular order to access key bits.
- Trap Bits may be present at any level of hierarchy.
- Trap Bits can affect a different TDR than the one they reside in.
- Unlocking multiple LSiBs requires determining which bits are the actual LSIBs and keys at each step.

% Increase in Expected Time for 2 LSIBs over 1 LSiB with Traps



k=# of key bits, n=number of bits in chain

Conclusions

- Simply breaking the JTAG port to protect embedded instruments can severely hinder debug & diagnosis.
- Locking SIBs hide instruments by using data naturally present in the P1687 network as keys.
- Even relatively small key sizes can greatly increase expected time required for attack.
- Traps significantly increase the cost of a guess.
- Hierarchical structures with multiple LSIBs help protect against lucky first quesses and increase complexity.
- Locks, Keys, and Traps are an especially important tool for preventing counterfeiting, IP theft, and the malicious (or inadvertent) destruction of hardware.

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