ASTER Technologies

Test Forum 2013

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- Good products
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- Manufacturing Defects
- Test Coverage
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DfX – Defect Universe & test coverage

They design defects, They manufacture defects, They sell defects. What about you?

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NTF Nordic Test Forum

TEST FORUM 2013

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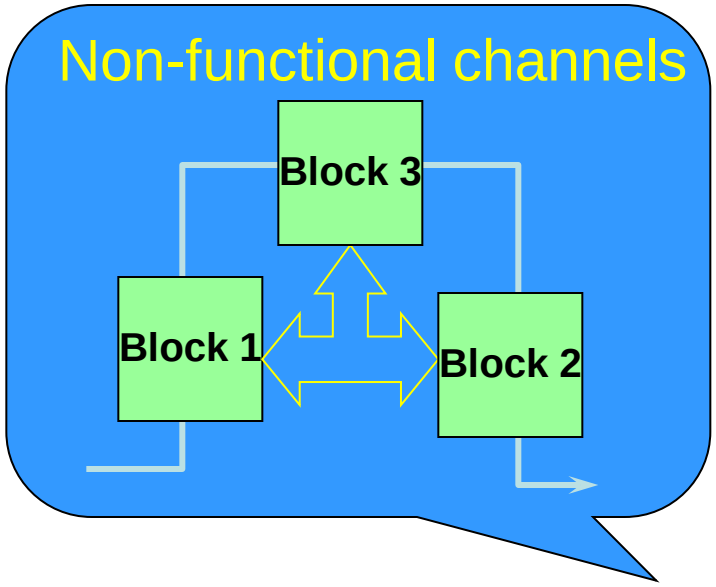
Design and production changes

- Functional complexity of electronic boards.
- Staggering board density.
- Outsourcing of board assembly.



SMD, fine pitch,
BGA, buried via

We buy good boards

We buy good boards

- Is a board good because it passes the test?
- What is the acceptable percentage of faulty boards that could be delivered with the “good boards” label?

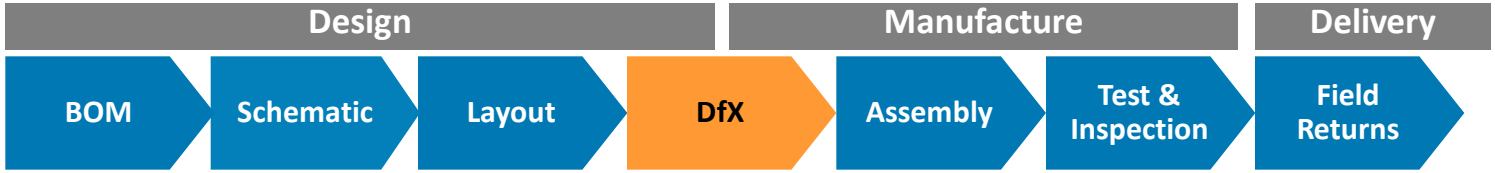
A man with one watch knows what time it is.

A man with two watches is never sure.

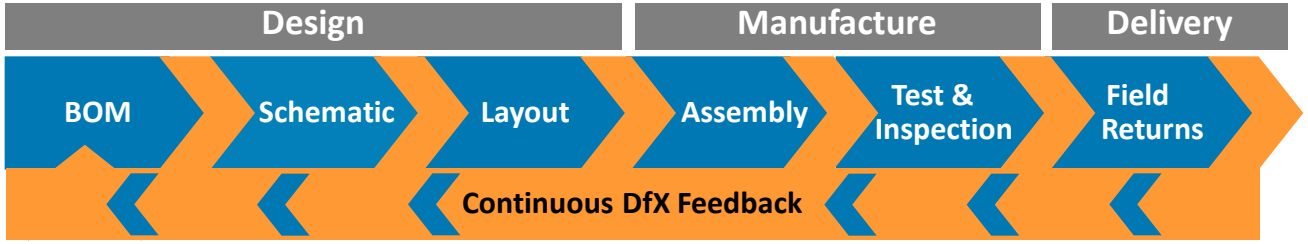
- Coverage must be readable from design to production : Unified metrics to compare & combine.

Design For Excellence

↳ Traditional Workflow: Expensive and Longer.



↳ TestWay - A unique dedicated workflow from Design to Delivery, where DfX is distributed.



Good products

- Good products must be defect-free at minimum cost.
- How to detect or prevent all faults on the product so that only good products are shipped?

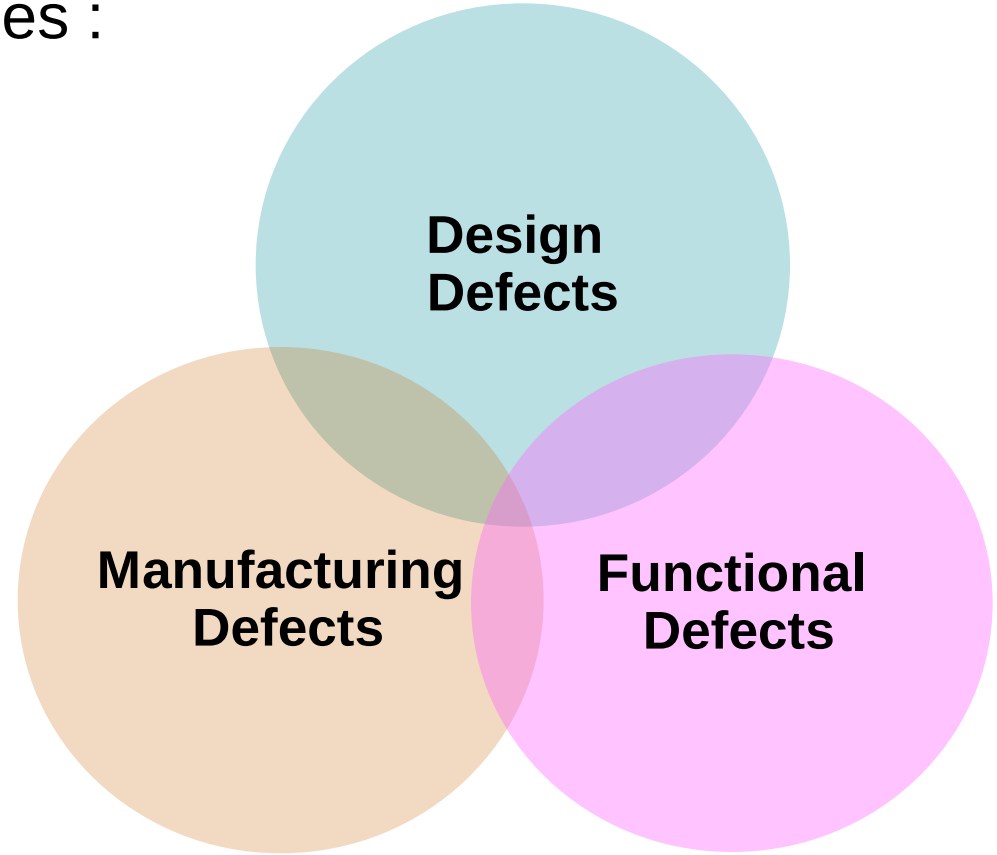
Defect Detection

Defect Prevention

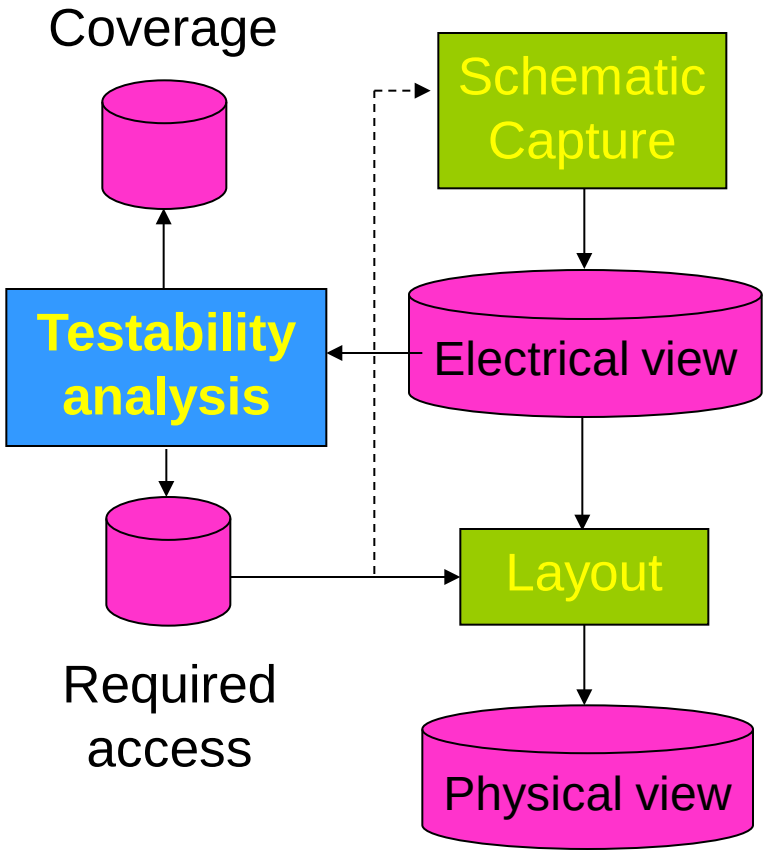
- Test coverage is a key metric as it will be the quality warranty and the main driving factor for LeanTest.

Defect Universe

- In order to consider all defects including design validation and testing, we need 3 main defect classes :

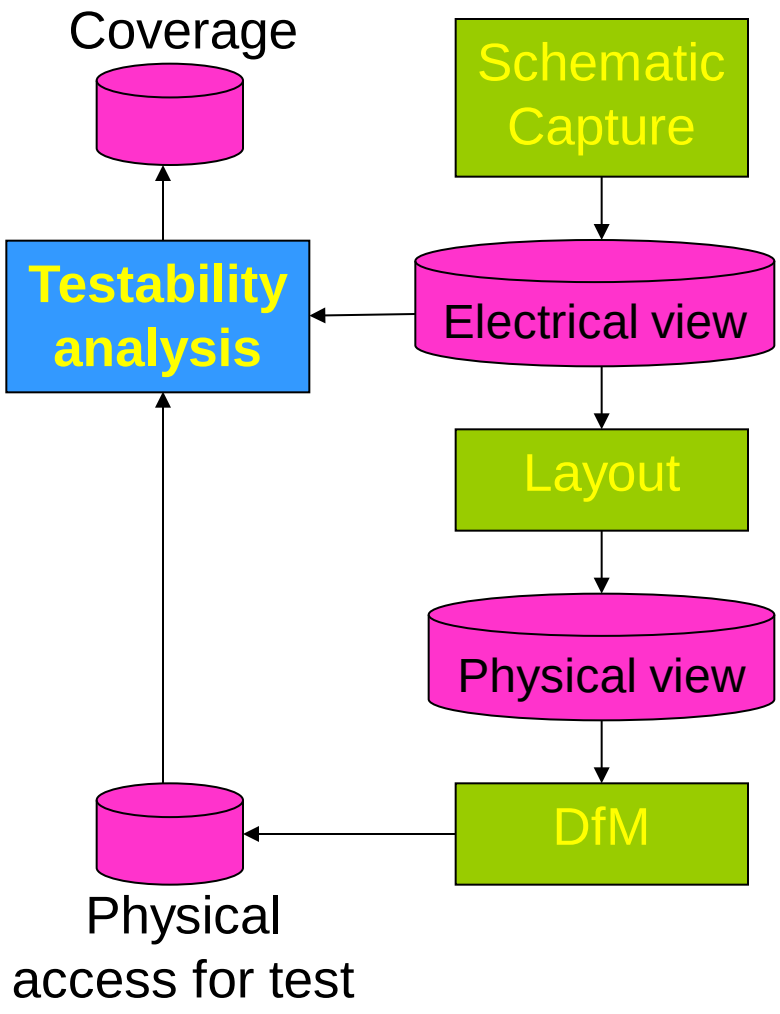


Schematic – Electrical DfT

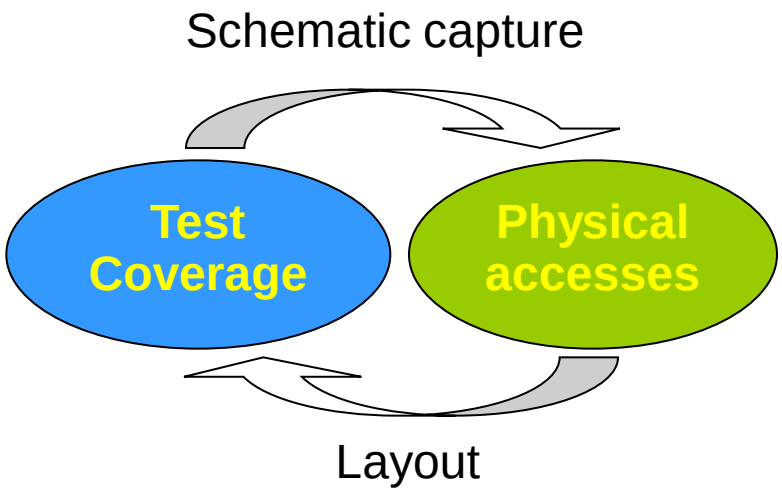


- Design and Testability rules violations limit test coverage.
- Accessibility requirements are back annotated prior to layout, ensuring that the required physical accesses will be available where they are mandatory.

Layout – Mechanical DfT



- The copper area having the required properties will be used as access points for In-Circuit Test or Flying Probe Test.



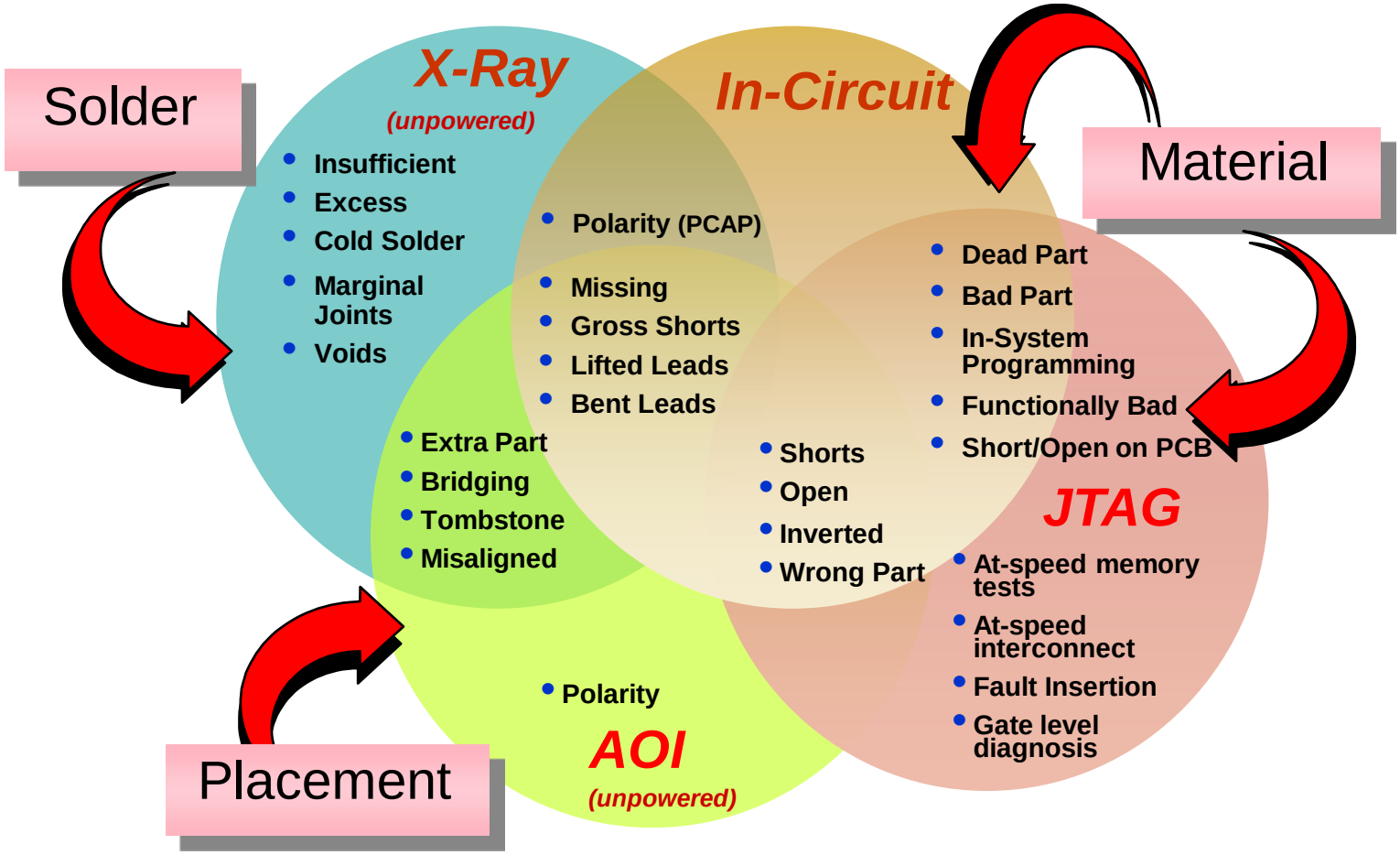
Test Coverage

- Demonstration using an absurd example
  - ✓ Board - 4 components: 3 resistors, 1 BGA.
  - ✓ The 3 resistors are measured with very high accuracy.
  - ✓ No test on the BGA.
  - ✓ Is the board test score really 75%?
    3 resistors / 4 components

  - ✓ We need something to weight the coverage… It must be credible, easy to update to reflect growing electronics complexity.

Manufacturing Defect Universe

- Identify the faults that can occur.



Manufacturing Defect Universe

- Typical manufacturing defects:

Missing components
Misalignment
Wrong value
Incorrect Polarity
Open Circuits
Broken components
Tombstone
Short circuits
Insufficient solder
Excessive solder

- We need to group defects into categories, to understand what defects can be captured by a particular test strategy.

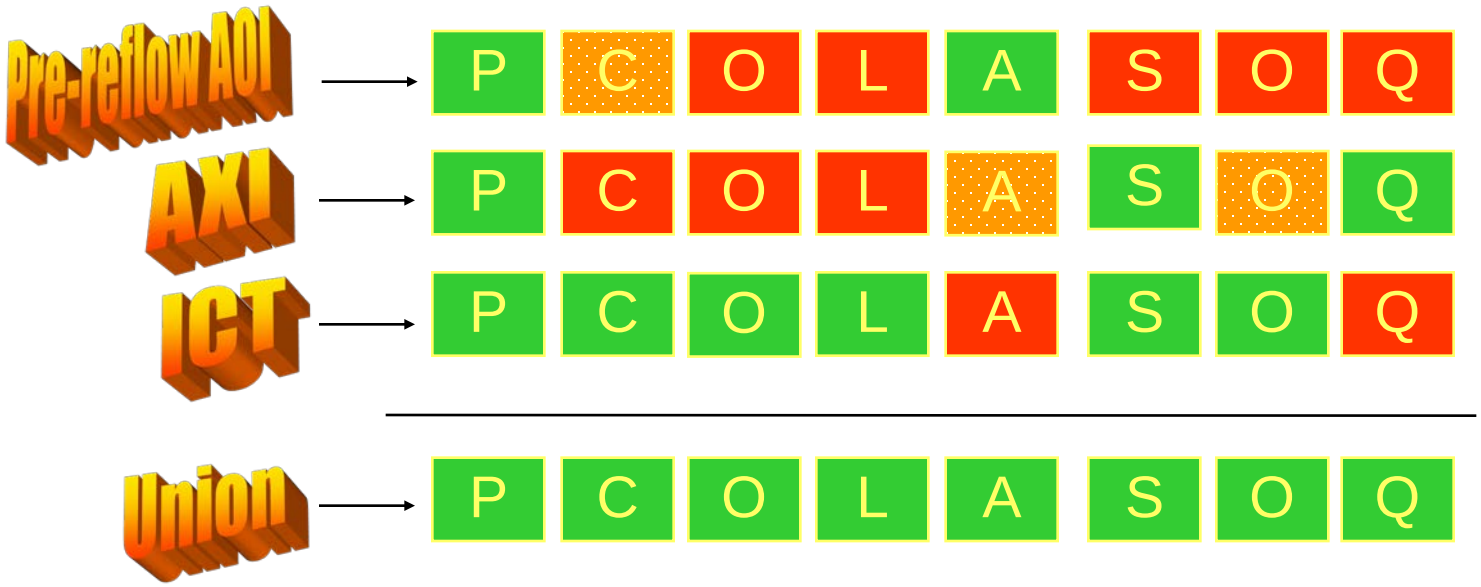
Test coverage

- The ability to detect defects can be expressed with a number: coverage.
- Each defect category fits with its test coverage:

MPSF [1]	PPVSF	PCOLA/SOQ /FAM
Material	Value	Correct
		Live
Placement	Presence	Presence
		Alignment
	Polarity	Orientation
Solder	Solder	Short
		Open
		Quality
Function	Function	Feature
		At-Speed
		Measure

Test coverage by defect category

- Each test technique brings a certain ability to capture the defect universe.
- No single solution is capable of detecting all the defects.



- Good coverage = combination of tests.

Test coverage by defect category

- For each category (Material, Placement, Solder) of defects (D), we associate the corresponding coverage (C).

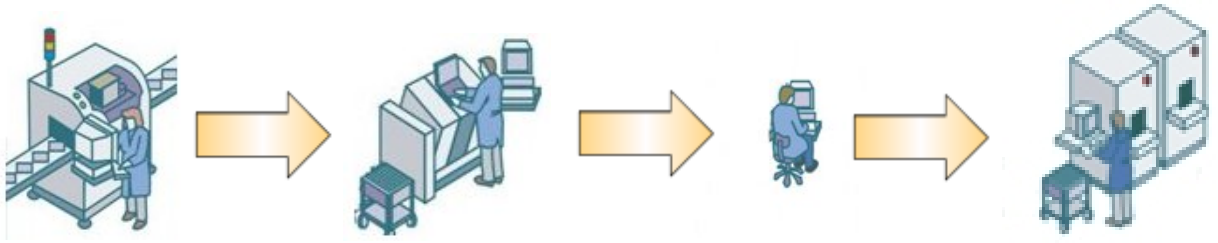
$$\text{Effectiveness} = \frac{\Sigma D_M \times C_M + \Sigma D_P \times C_P + \Sigma D_S \times C_S + \Sigma D_F \times C_F}{\Sigma D_M + \Sigma D_P + \Sigma D_S + \Sigma D_F}$$

- The test efficiency is based on a coverage balanced by the defect opportunities.

We need a better coverage where there are more defect opportunities!

Faulty boards at system level

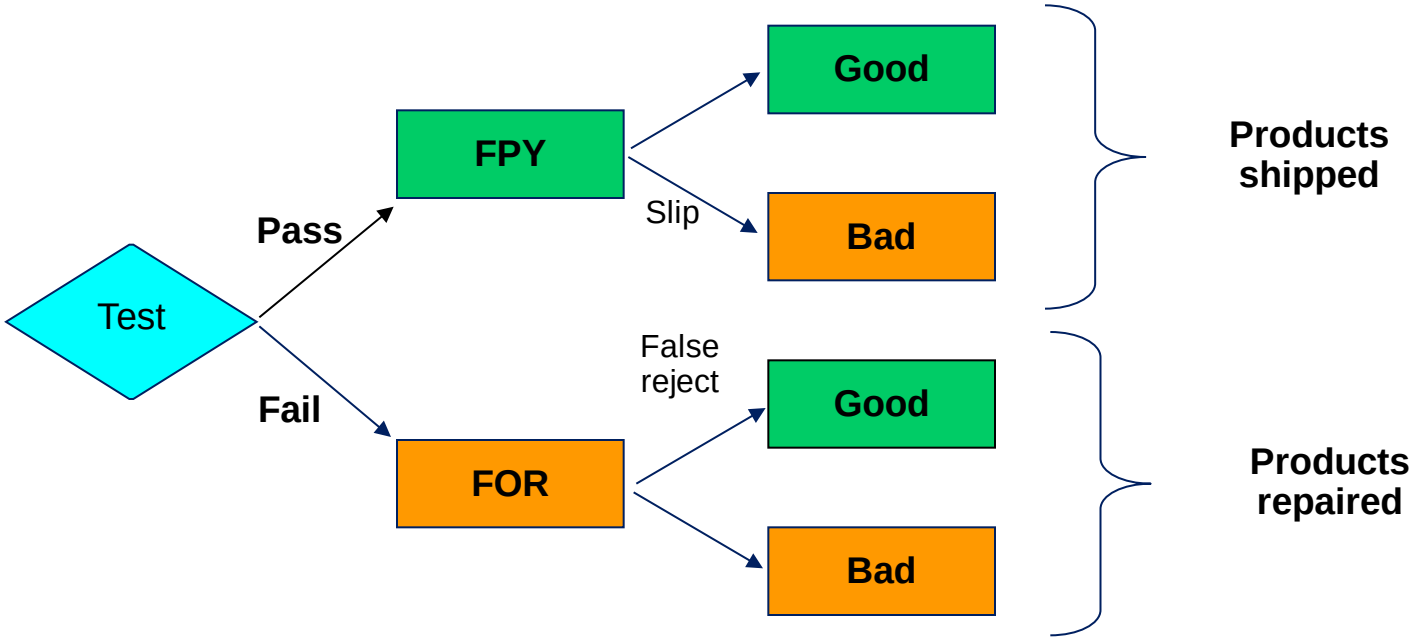
- Electronic plants, in charge of board integration, often discover a significant amount of defective boards at system test.



- How is it possible to get failures at system level if we only buy good boards?
  - ? The defect appears during packing and transportation (vibration, extreme temperatures, moisture).
  - ? The defect is a dynamic problem which is revealed by the integration of the board in the complete system.
  - ? The reality is usually more simple…

Faulty boards at system level

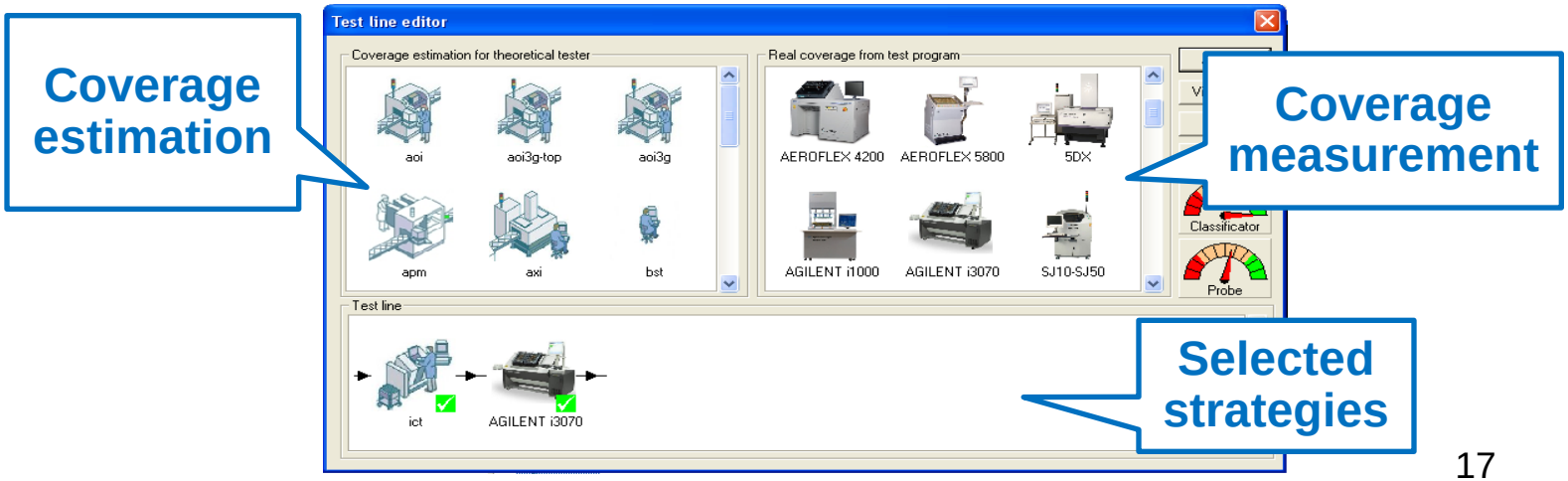
- If the board is failing at system test, it is usually because the escape rate (or slip) is higher than expected.



- There are only two possibilities:
  - ✓ The combined coverage is lower than optimal.
  - ✓ The DPMO figures are higher than expected.

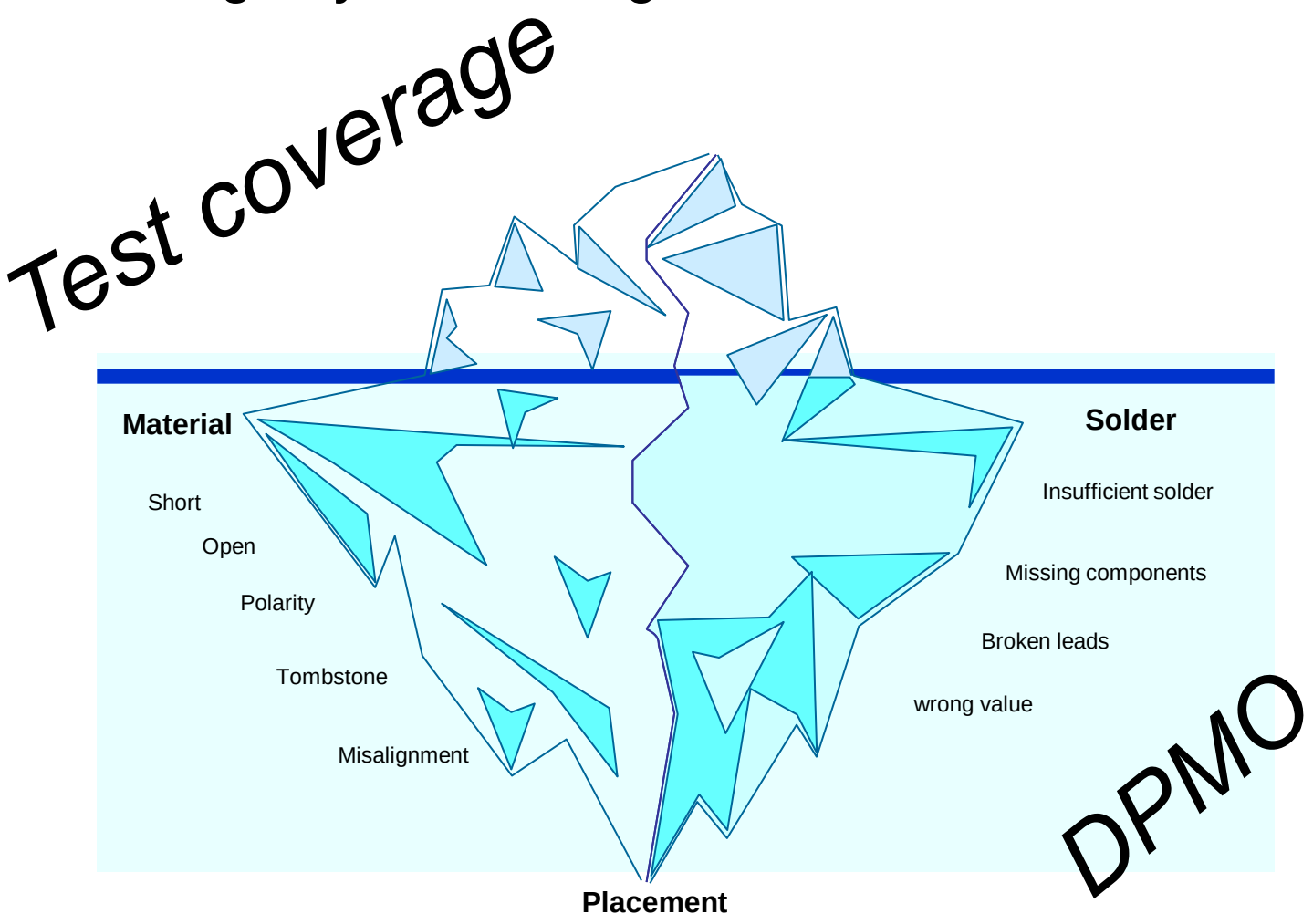
Faulty boards at system level

- The auditing conclusions were:
  - ✓ Wrong or inadequate coverage metrics are produced: Example: confusion between accessibility and testability; coverage by component only - without incorporating solder joint figures ; Over optimistic report (marketing driven report),
  - ✓ Wrong DPMO figures, due to limited traceability or incorrect root cause analysis (Example: confusion between fault message and root cause/defect).



DPMO estimation

- Going beyond solving surface issues.



Conclusion

- From design, during production and in a more general way, through the whole life cycle, coverage estimation permits the test process to be optimized.
- By deploying various testers in the best order, at the best time, with controlled levels of redundancies, costs can be reduced and quality levels raised.
- The economic challenges are critical: the tools to meet them are available

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